

A Low-Cost, Low-Power Wireless Receiver

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Outline

- Motivation
- Introduction to Specifications Design
- Signal Path Design and Experimental Verification
- Synthesizer Design and Experimental Verification
- Final Receiver Design and Measurements

Motivation

Eliminate wires everywhere !



Basic System Requirements

- Data rate: 1 Mb/s.
- ISM band operation.
- A few channels (>5) for diversity/ multiple access.
- Robust modulation scheme.
- Range ~ 10 m.
- Implementable with very low-cost, low-power devices.

One Solution: Bluetooth

- State-of-the-art CMOS Bluetooth Radio (Ericsson, ISSCC 2002)

Data Rate: **1 Mb/s**

Active Receiver Current = **30 mA**

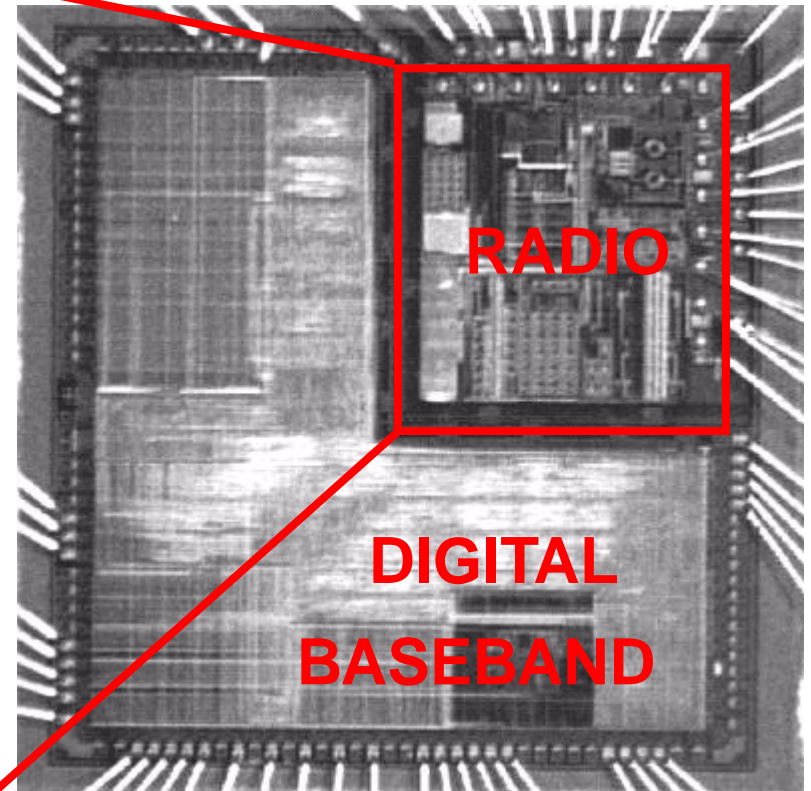
Active Transmit Current = **35.5 mA**

Supply Voltage ~ **2.5 - 3 V**

Active Radio Area = **4.0 mm²**

Technology: **0.18 μm CMOS**

Offchip: **Loop filter, SAW filter**



Can we make some tradeoffs at the system level to lower costs?

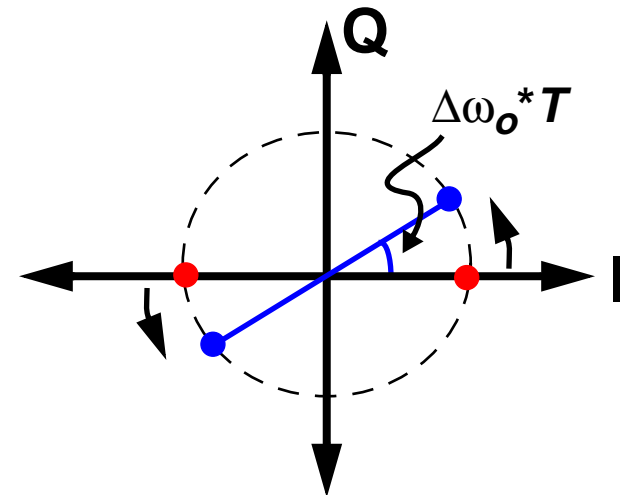
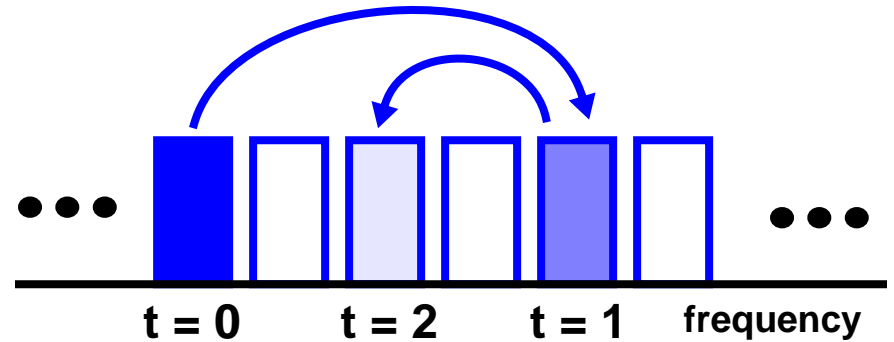
Build a Simple System (I)

	Bluetooth	Zigbee	Zero-G
Data Rate	1 Mb/s	250 kb/s	1 Mb/s
Spreading	FHSS, 79 Chan.	DSSS, 32-chip PN code	DSSS, 10-chip offset code
Modulation	BFSK	O-QPSK	DBPSK
Crystal Offset Tol.	20 ppm	80 ppm	200 ppm
Pulse Shaping	Gaussian	Half sine	Gaussian
Sensitivity	-70 dBm	-85 dBm	-75 dBm

- **A new approach - concurrent design of circuits and system specifications.**

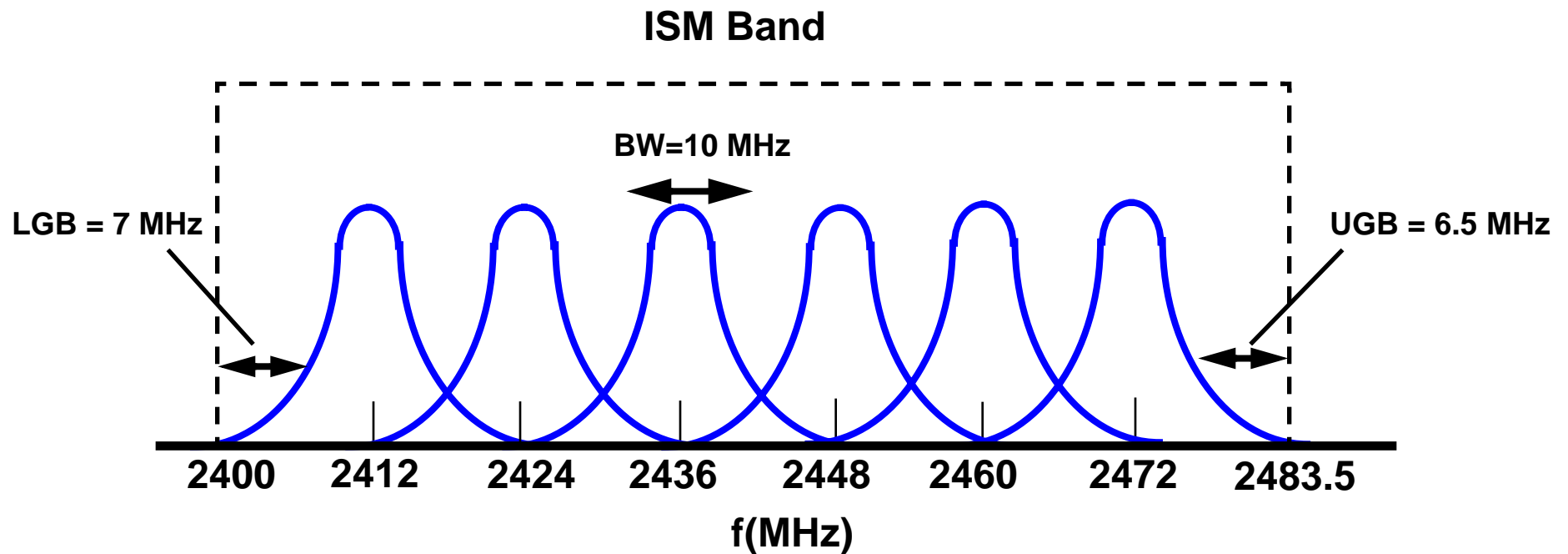
Build a Simple System (II)

- Choose **direct-sequence spreading (DSSS)**: Frequency Hopping (FHSS) places strict requirements on PLL settling time.
- **Differential phase-shift keying (DPSK)**: robust to crystal frequency offset.



Build a Simple System (III)

- Choose channels: $2400 + 12n$ MHz, $n = 1..6$.

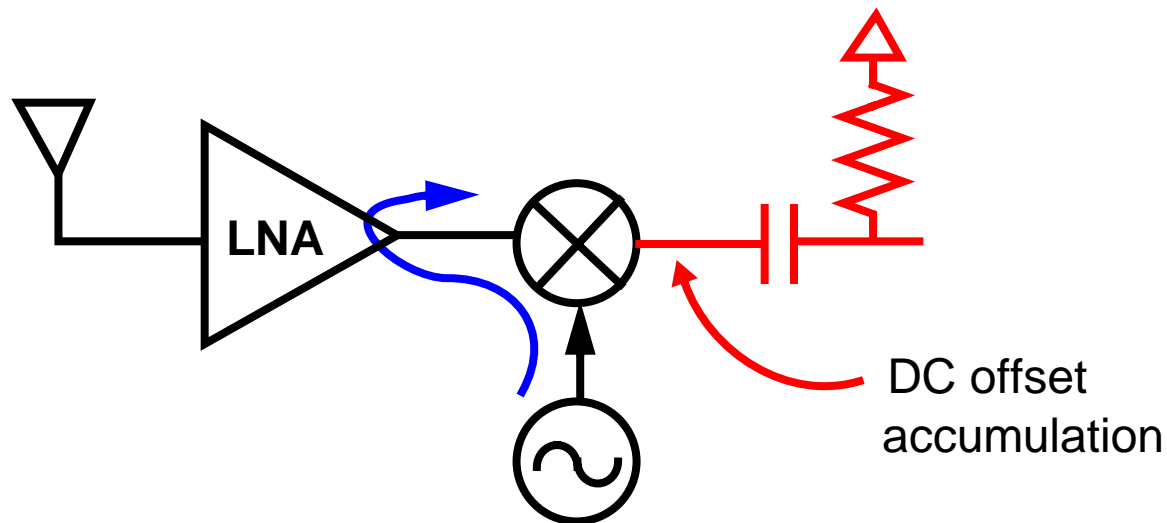


- Relax oscillator phase noise requirement by using large inter-channel spacing and guard bands.

Spectrum Shaping: Offset Coding (I)

- Choose **direct conversion**: low-power, area-efficient radio architecture.
- DC offset problem at output of mixer. Simple solution: Use large DC-blocking capacitor.

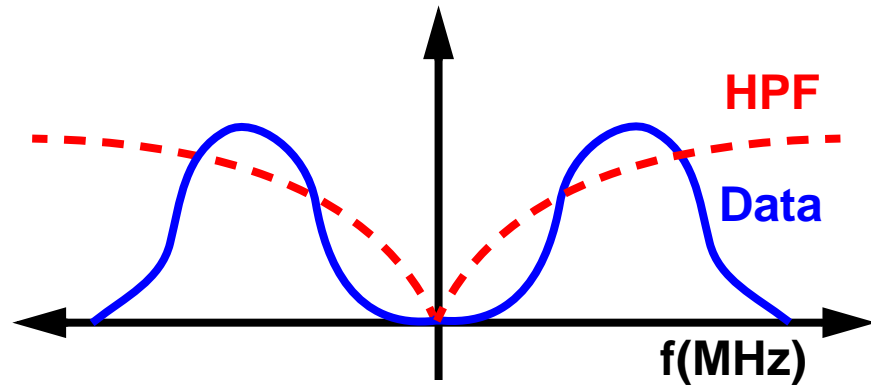
Problem : large capacitor for low cutoff frequency, low noise.



Spectrum Shaping: Offset Coding (II)

- **A solution:**

Shape the spectrum away from DC using coding- allows smaller capacitor size.



- Additionally, we must use differential encoding for robustness to oscillator frequency offset.

Spectrum Shaping: Offset Coding (III)

- Example: **4-bit case DC-free spreading case**
- Let **(1101)** and **(0010)** be spreading symbols for **0** and **1**, resp.

If previous bit is **0**

DC-free diff. encoded sequences: **(1001)** and **(0011)**, resp.

If previous bit is **1**

DC-free diff. encoded sequences: **(0110)** and **(1100)**, resp.

- Independent of data, ... **xxx1xxx0xxx1xxx0** ... pattern appears.
- **Sharp tones - hard to meet FCC bandwidth requirement.**

Spectrum Shaping: Offset Coding (IV)

- Our solution - introduce periodicity in spreading sequence.
- Example: 4-bit DC-free spreading case
- Let **(1010)** and **(0111)** be spreading symbols for **0** and **1**, resp.

If previous bit is **0**

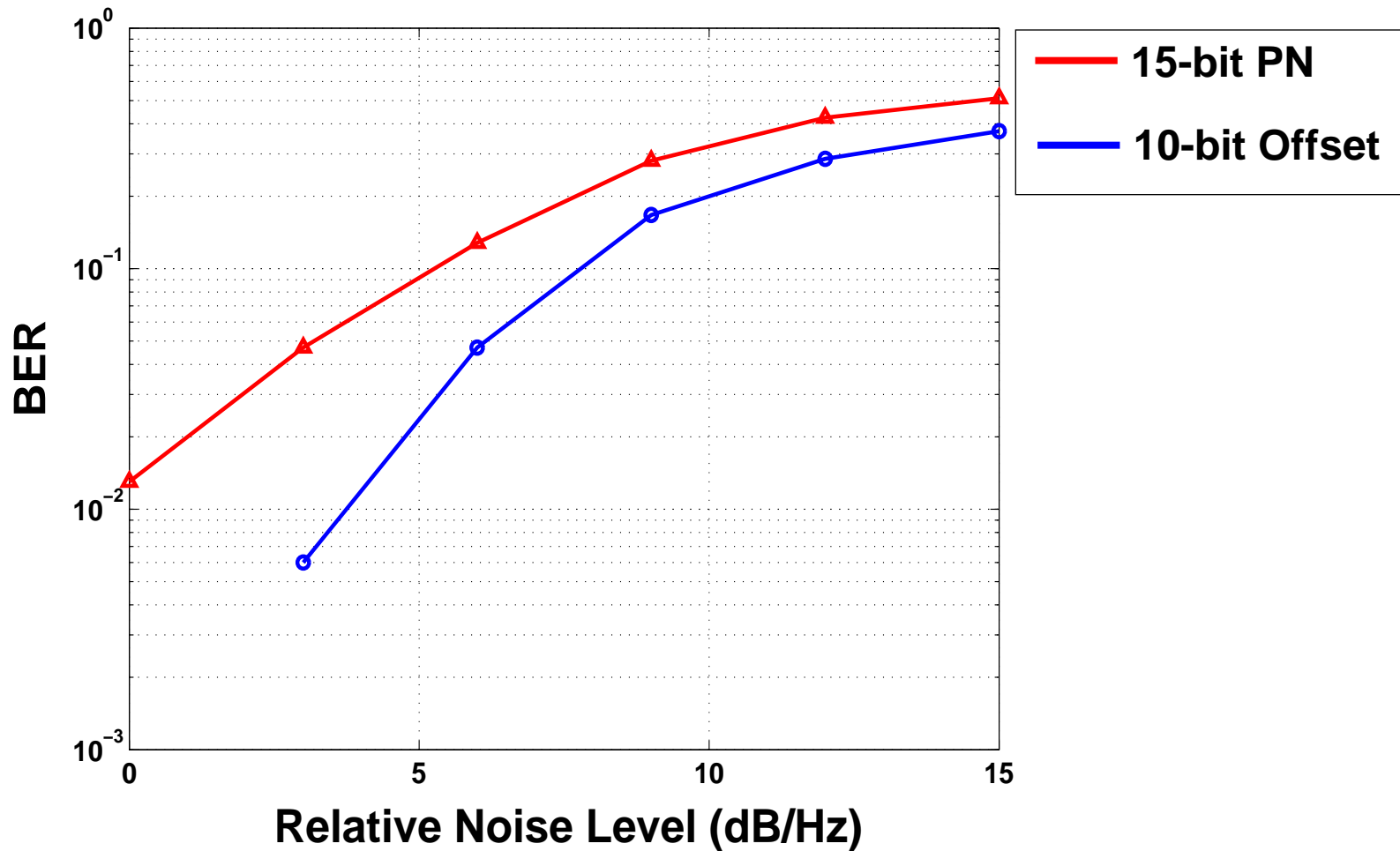
Diff. encoded sequences: **(1100)** and **(0101)**, resp.

If previous bit is **1**

Diff. encoded sequences: **(0011)** and **(1010)**, resp.

- Find such codes which minimize power close to DC.

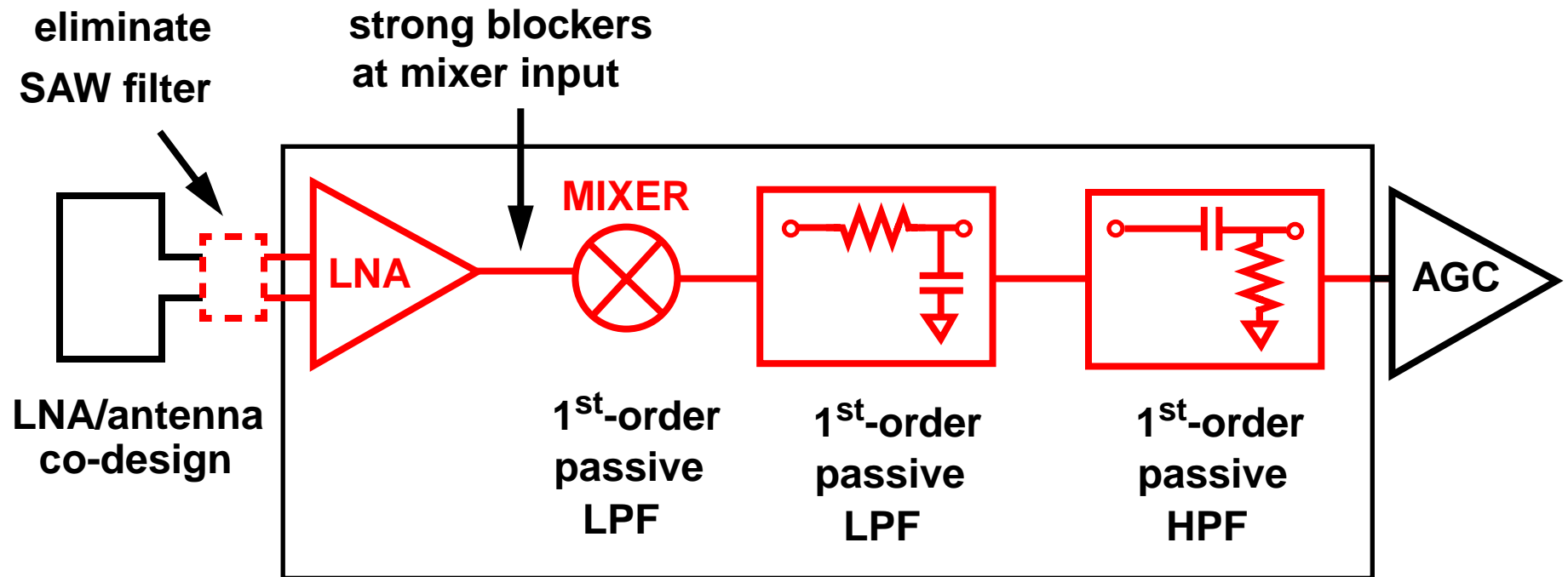
Offset Vs. PN codes : Simulated BER



- Chip rate = 10 Mchips/s, 500 kHz HPF, $N = 1000$ samples.

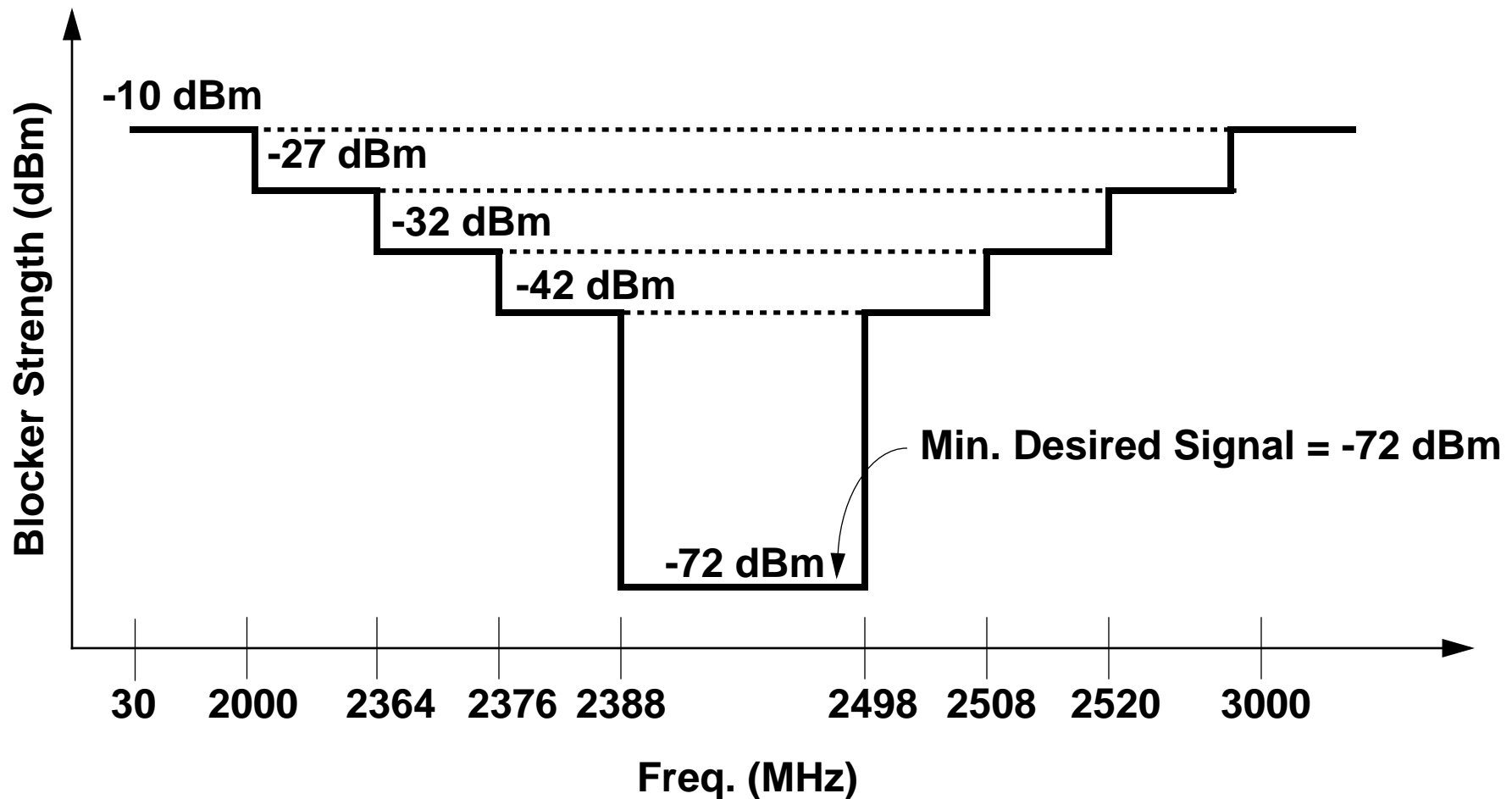
Receive Signal Path

- Front-end circuits:
 - robust to strong out-of-band blockers
 - acceptable noise performance with low power consumption

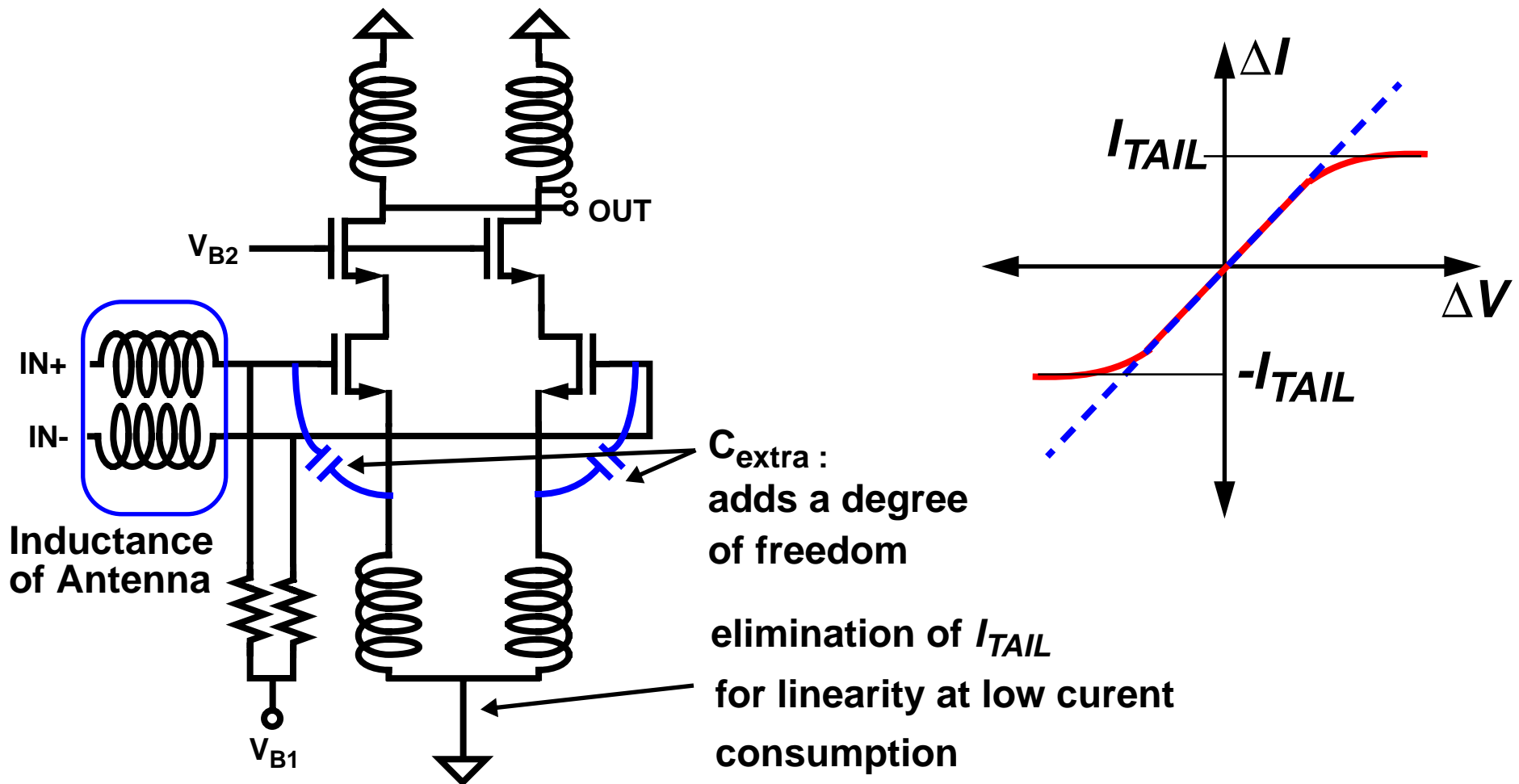


Receiver Out-of-band Blocking

- Strong signals expected 500 MHz away (from Bluetooth spec.)
- Eliminate off-chip RF preselect filter: linearity and filtering hard.

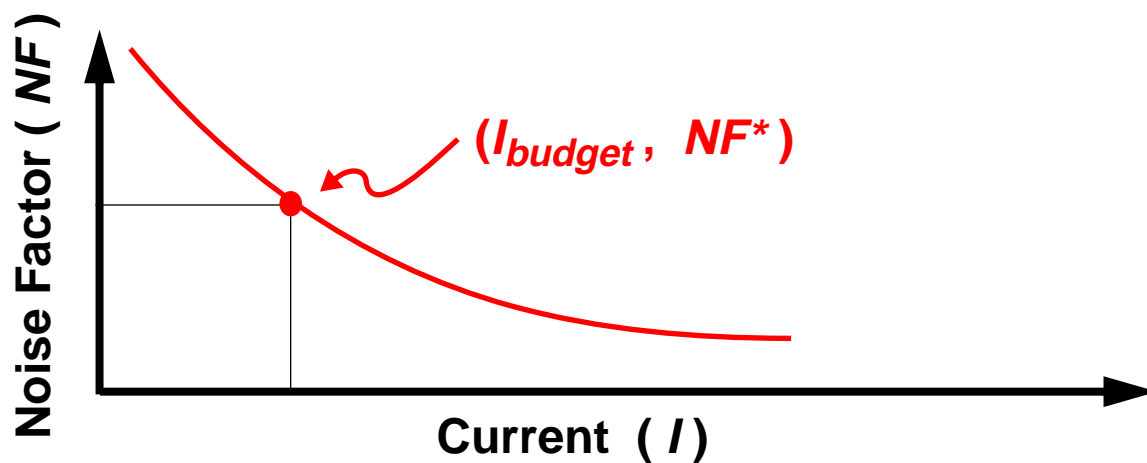
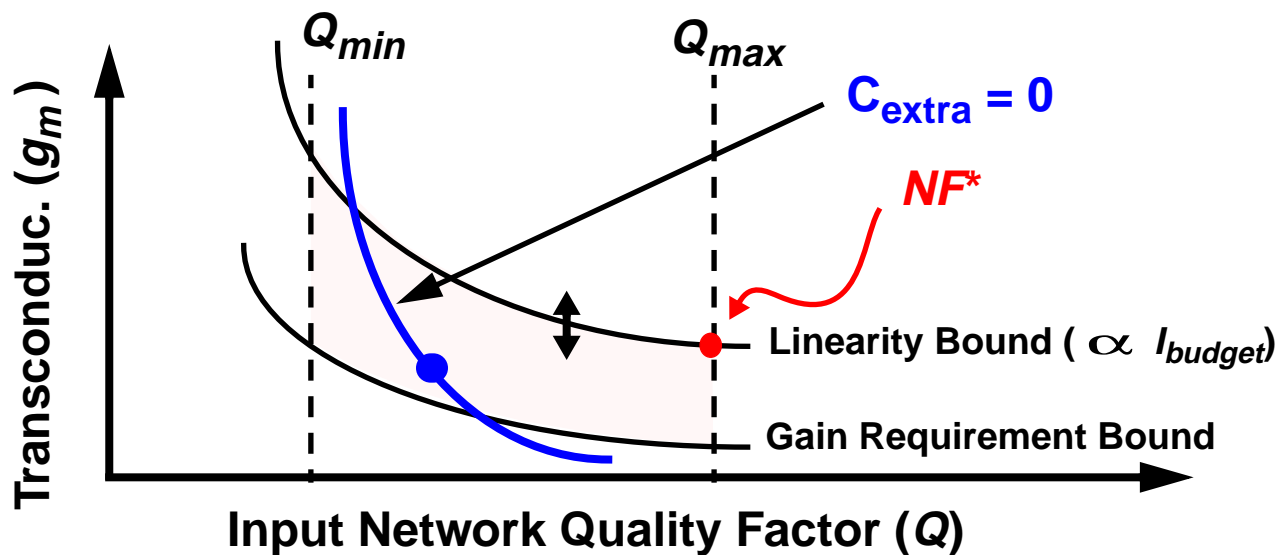


Low Noise Amplifier (I)



Andreani et al., "Noise optimization of an inductively degenerated CMOS low noise amplifier", *IEEE TCAS II*, vol. 48, pp. 835-841, Sept. 2001.

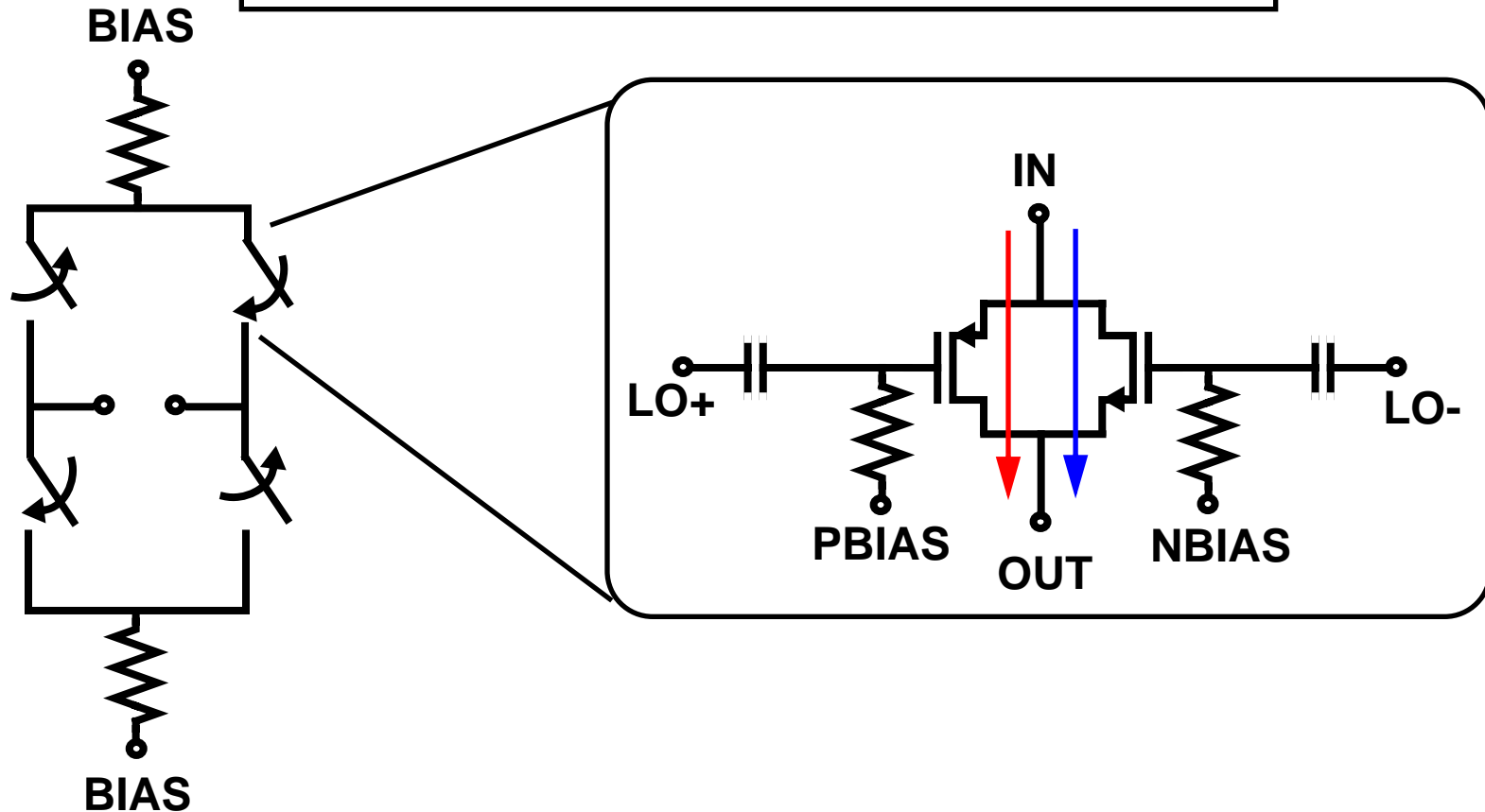
Low Noise Amplifier (II)



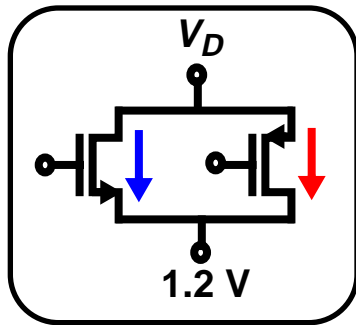
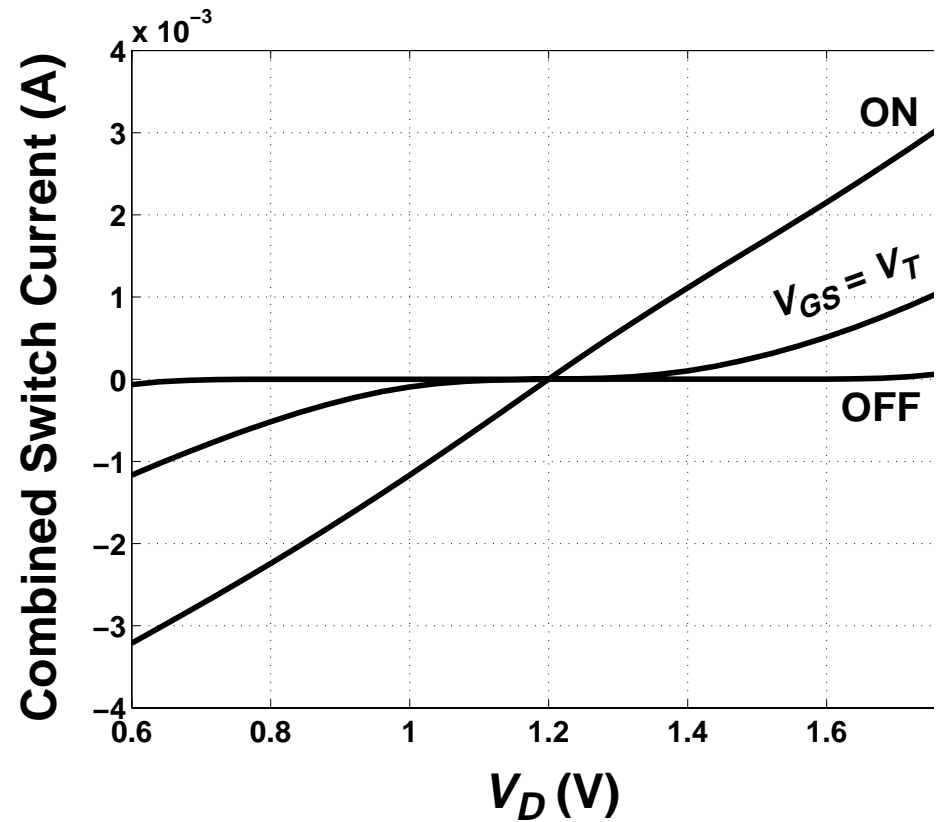
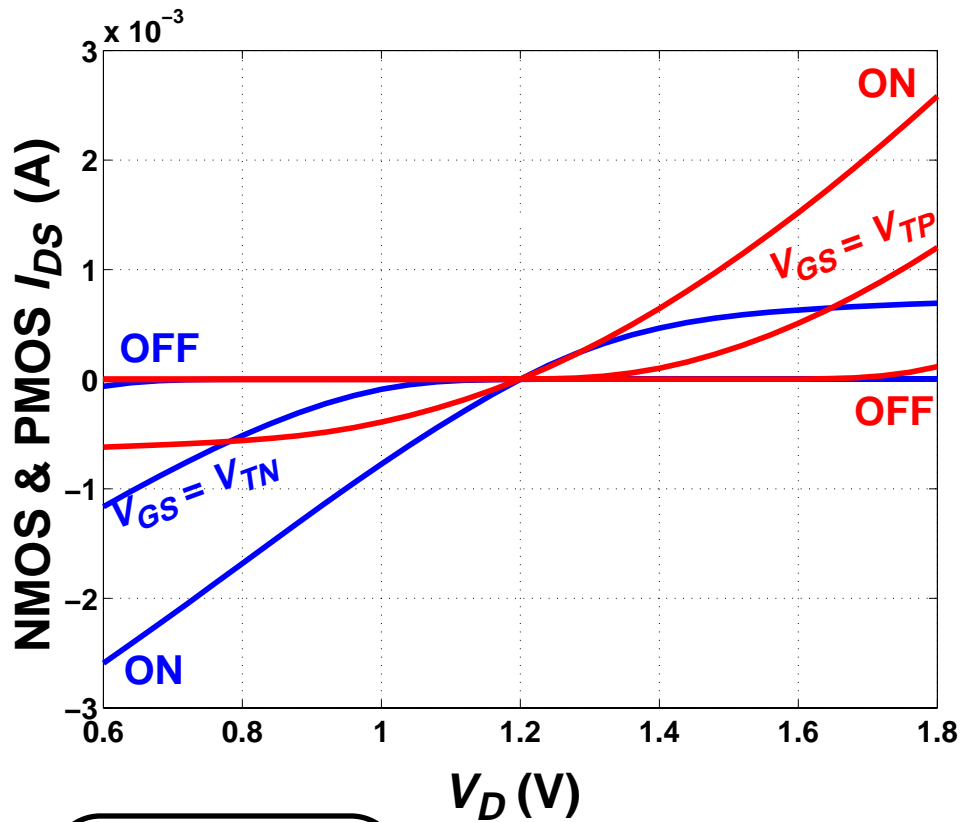
X-Gate Mixer (I)

- Need greater linearity in presence of strong blockers.
- Expensive to generate very large LO swings at RF.

Our solution: a mixer with x-gates

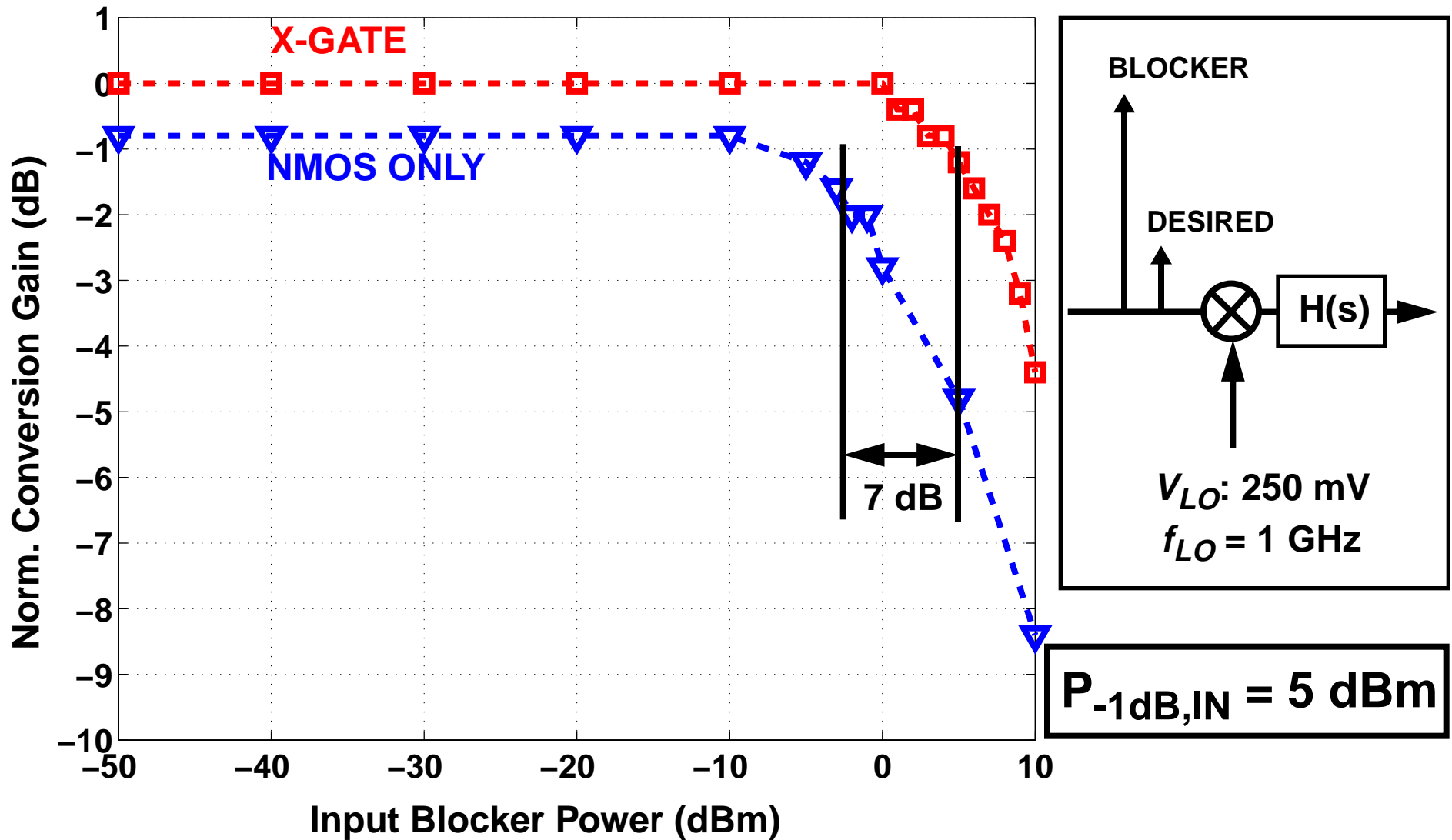


X-Gate Mixer (II): DC Simulations

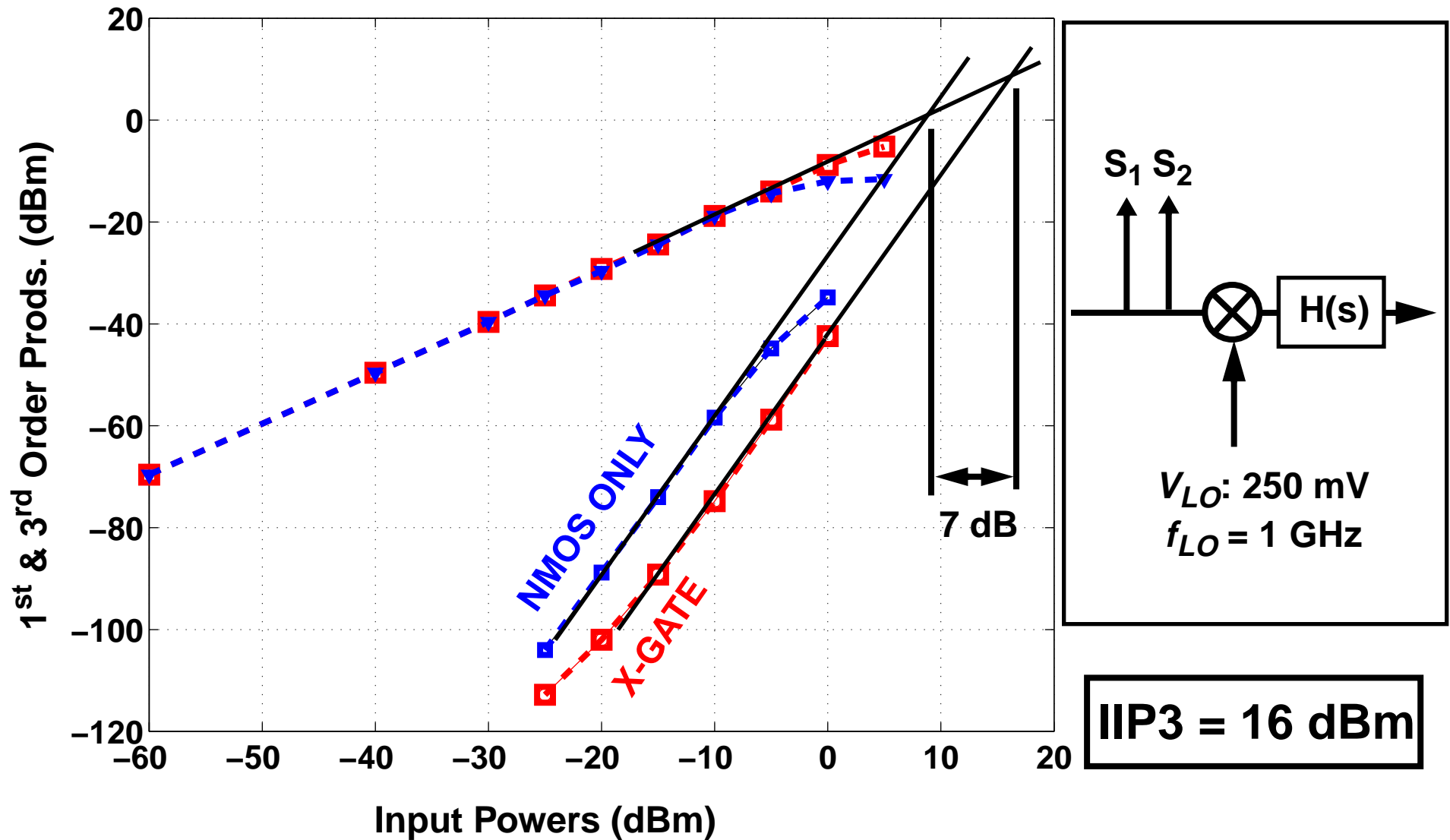


Mixer Linearity: Measurements (I)

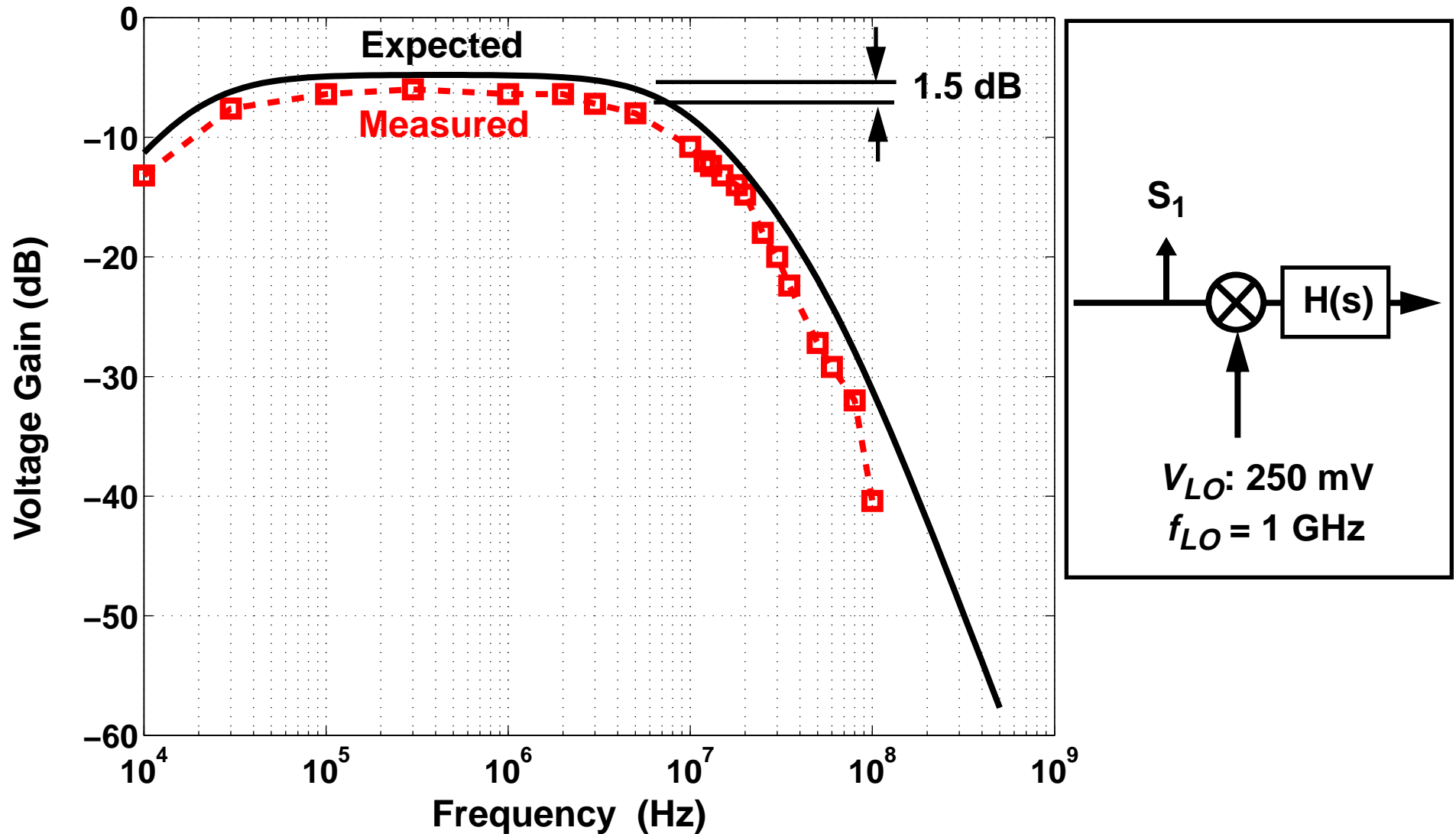
- Prototype mixer & filters built in 0.25 μm CMOS, tested at 1 GHz.



Mixer Linearity: Measurements (II)



Passive Chain: Measurements

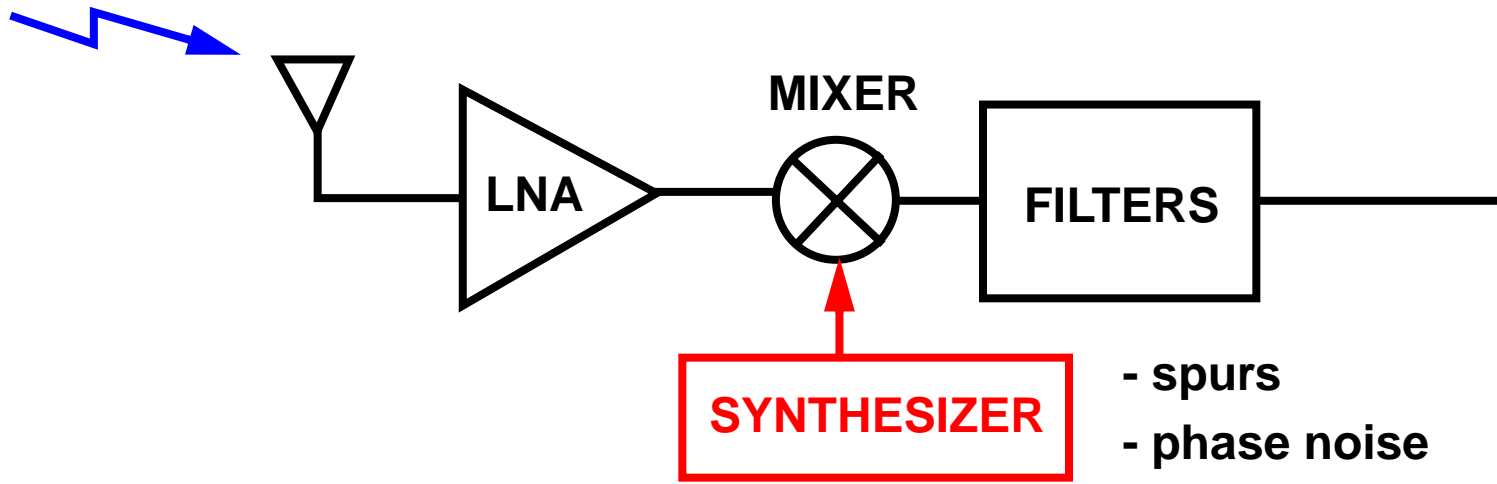


Receive Path Design Summary

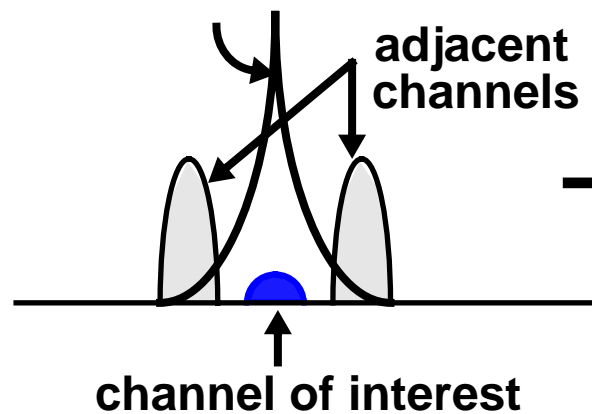
- A direct conversion architecture with simple HPF is utilized.
- Offset coding is introduced with differential encoding for spectral shaping.
- The expensive pre-LNA band-select filter is eliminated.
- The X-gate mixer is introduced for linear downconversion.
- A passive chain is utilized for filtering blocker signals post down-conversion.
- The passive receive chain (including mixer) has been fabricated and tested at 1 GHz.

Low-Power Frequency Synthesis

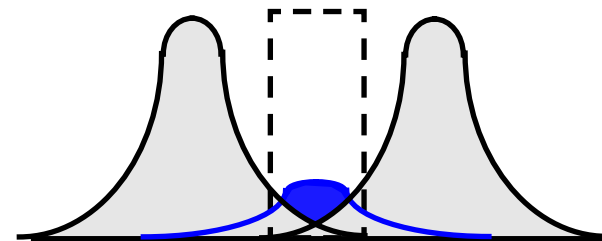
- A critical analog block ...



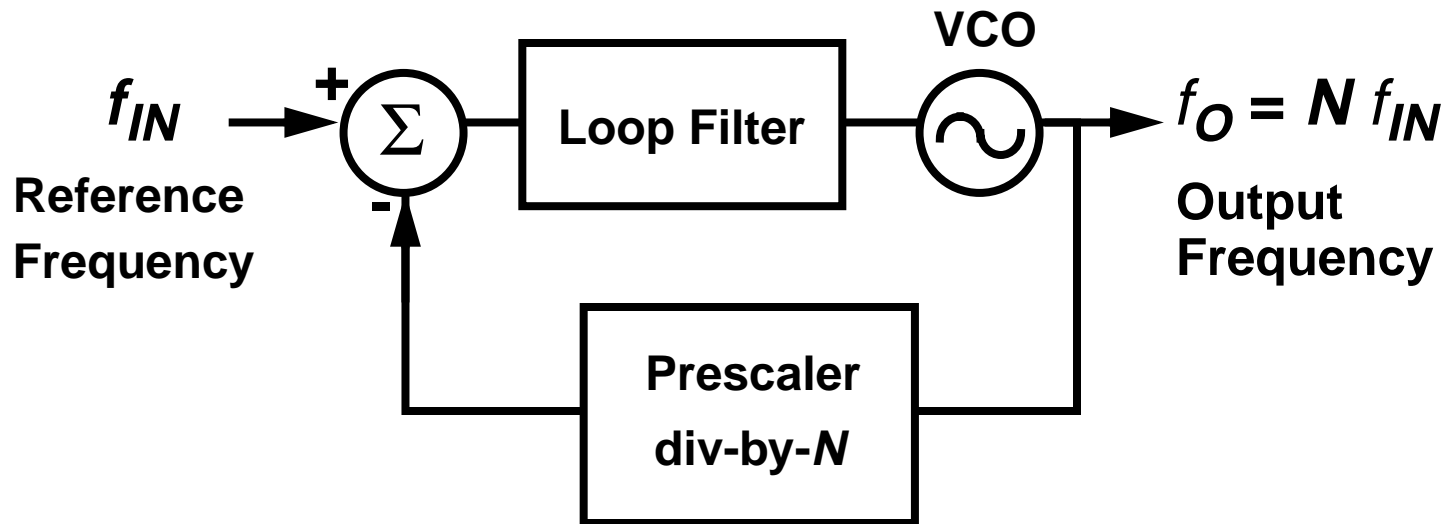
spectrum of local oscillator



downconverted spectrum



A Typical Frequency Synthesizer



- High frequency $f_O = N f_{IN}$ generated because of prescaler.
- Loop filter determines the dynamics of the loop.

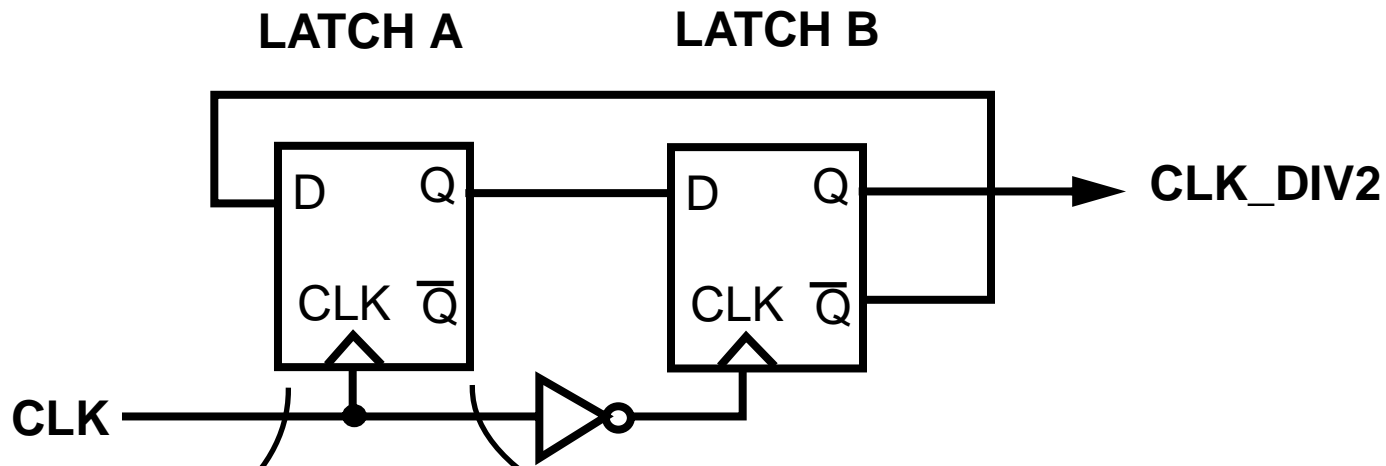
Power in Prescaler

- One major source of power consumption: high-frequency prescaler in the synthesizer.



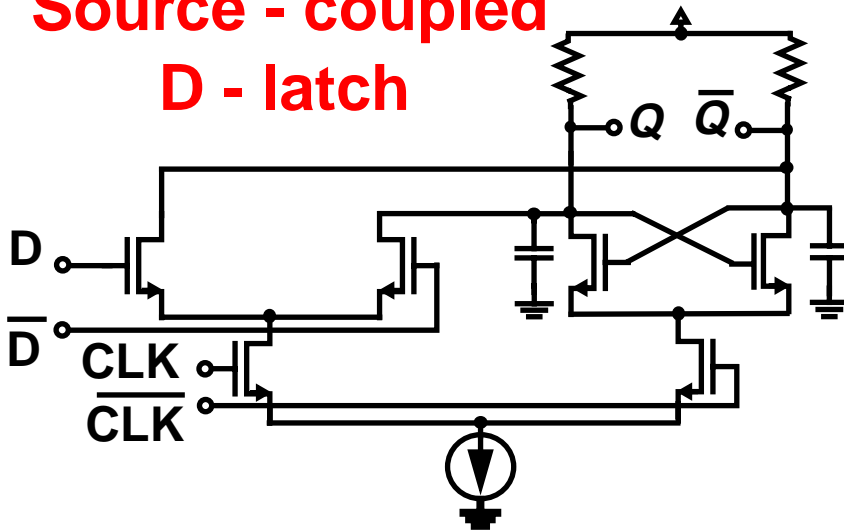
- Regular CMOS digital gates: Power scales as fCV_{DD}^2 .
- How to deal with the high-frequency divider?

Divide-by-2 in Low-Swing Logic



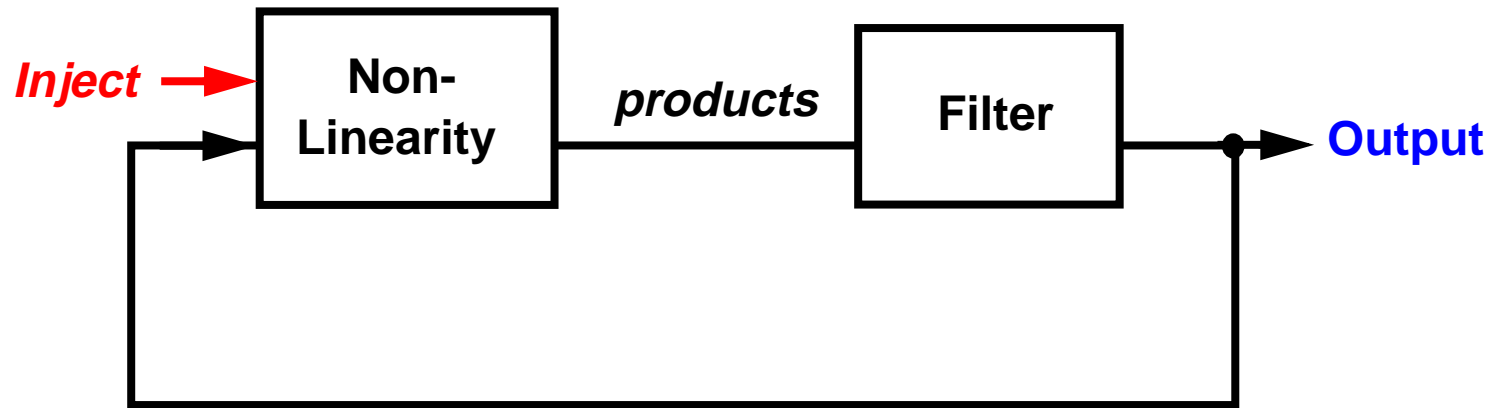
- lower power consumption $fCV_{DD}V_{swing}$, but f remains.

Source - coupled D - latch



Analog Regenerative Dividers

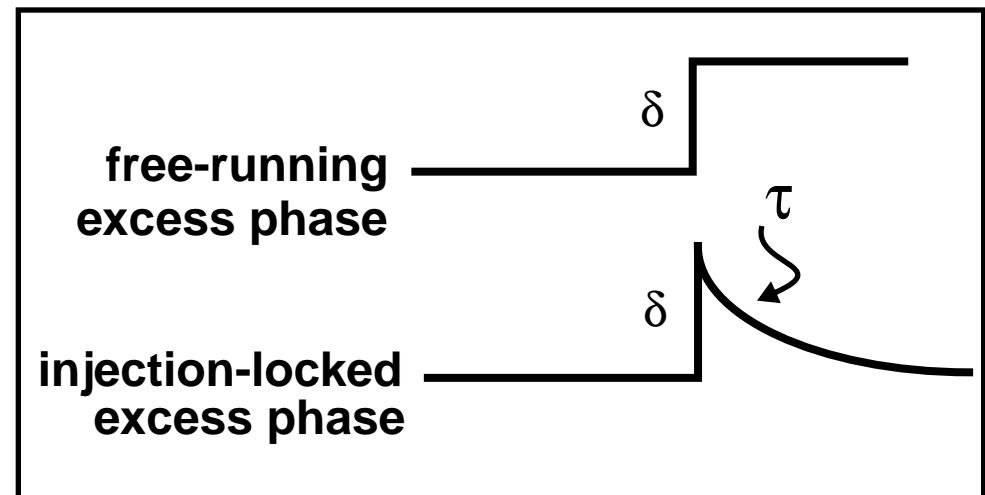
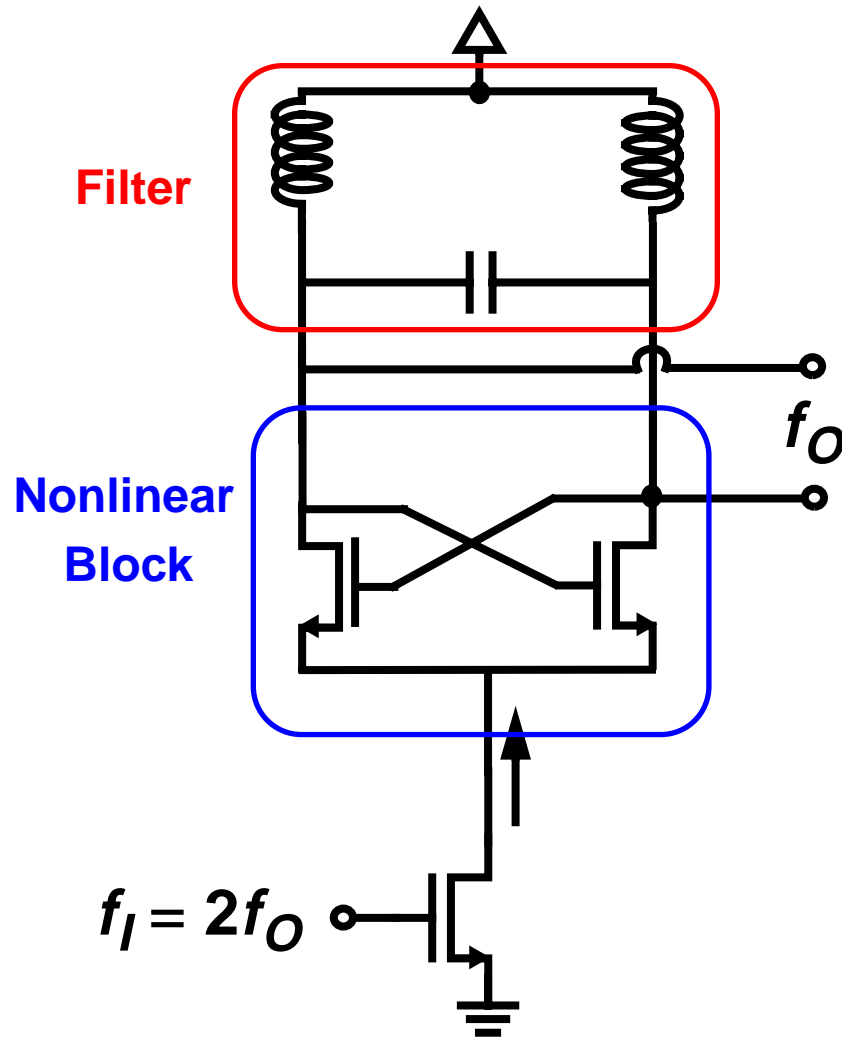
- Analog frequency dividers have power $V_{DD}I_{BIAS}$.



- If loop gain is sufficient without injection, feedback system oscillates at $f_{free-run}$.
- Regenerative system tracks f_I , the injection frequency/phase over some locking range. f_I must be close to $f_{free-run}$.

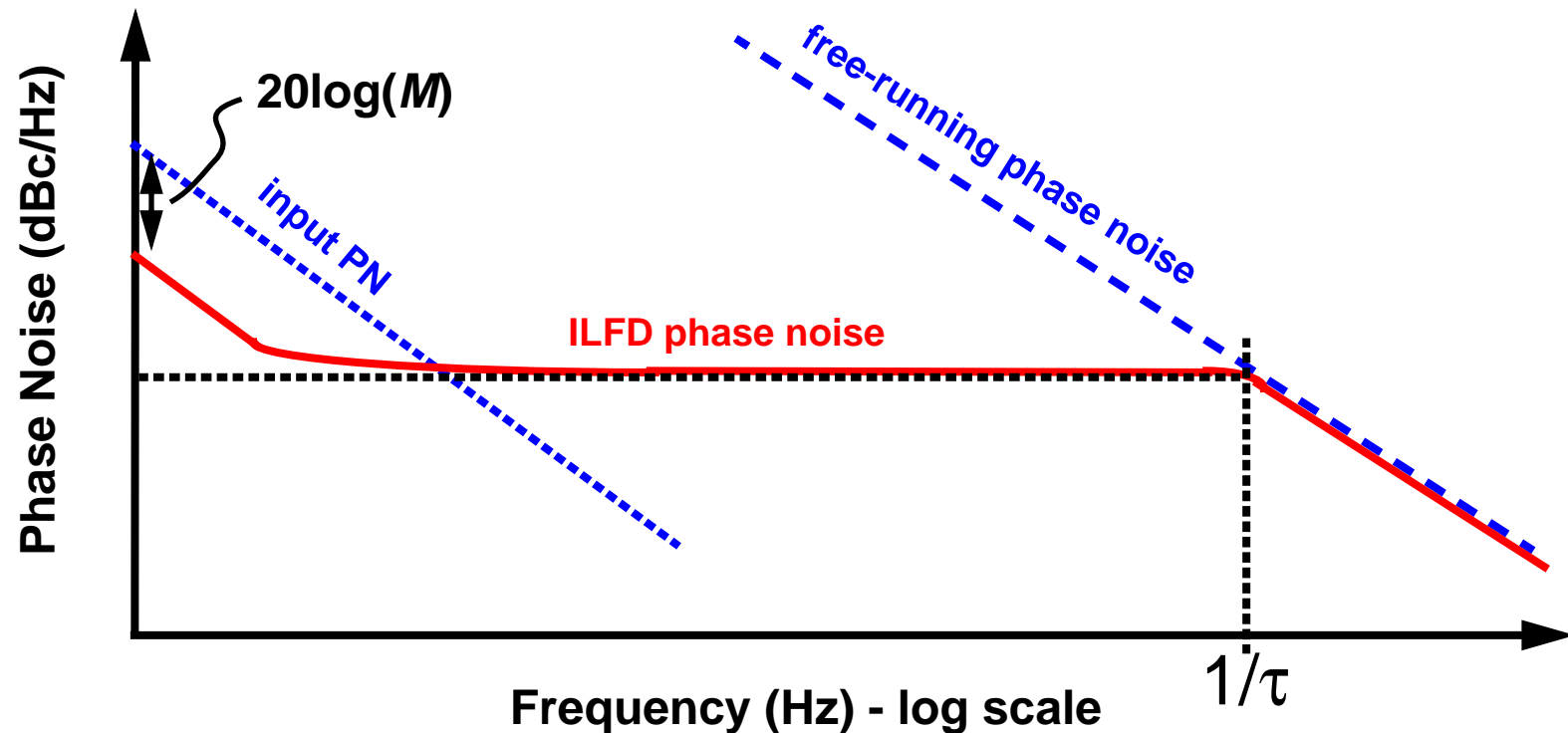
Injection-locked Frequency Divider

- A harmonic of $f_{free-run}$ can also be injected : system is a phase-locked divider.



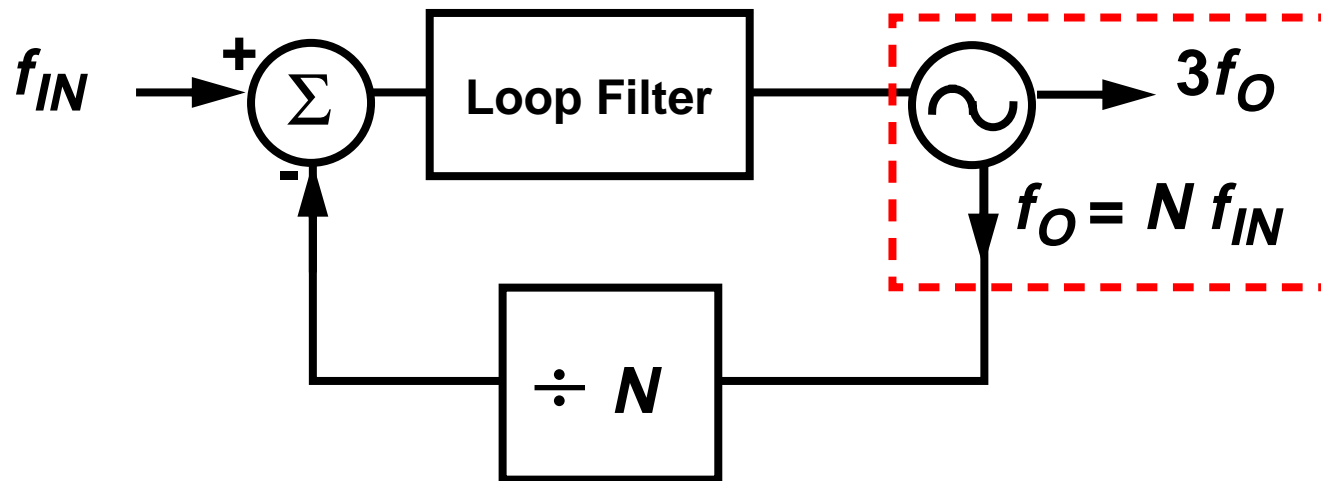
Phase Noise of ILFD

- Characteristic first-order time constant τ : determines the dynamic response, locking range and phase noise of the ILFD.

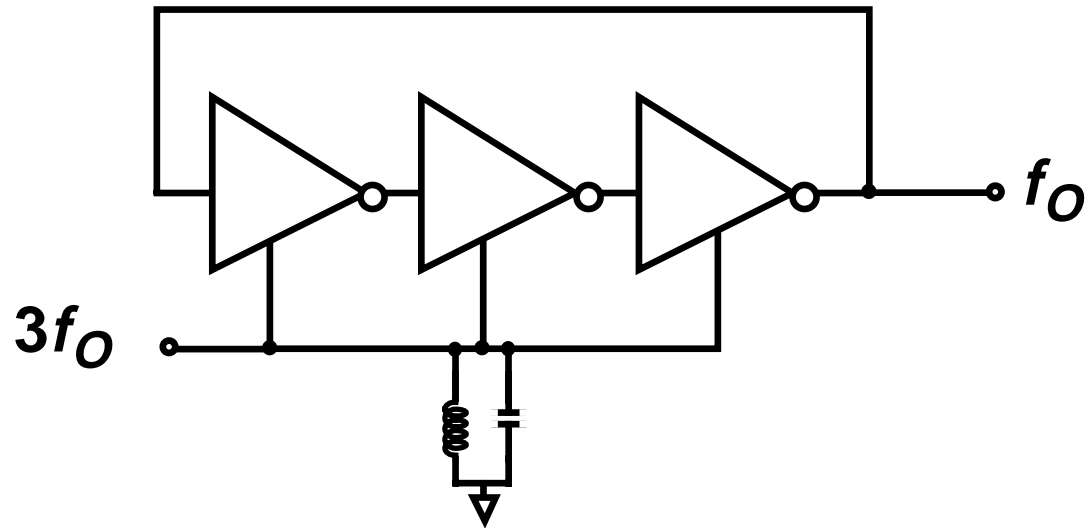


A New Oscillator

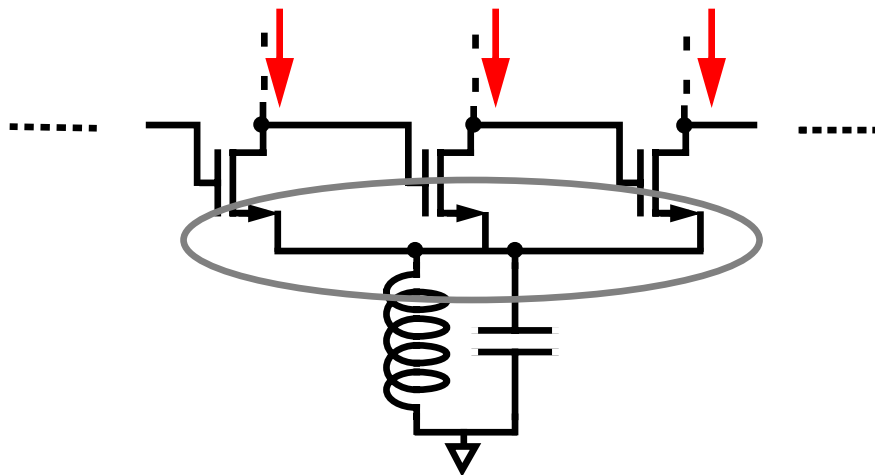
- We can do even better: eliminate a divide-by-3 circuit at the high-frequency end.
- Oscillator has two outputs: one at $3f_O$, and one at f_O .



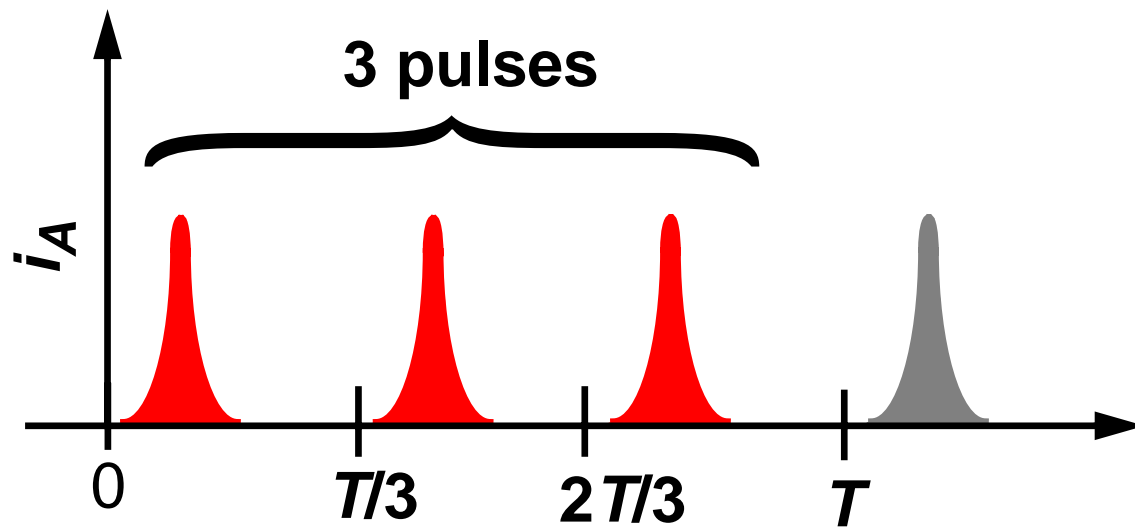
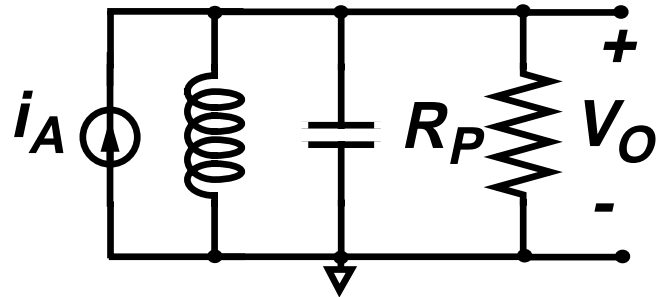
A Multiply-by-3 Ring Oscillator



- Currents from all stages of the ring are injected into the LC tank and combine to generate $3f_0$.

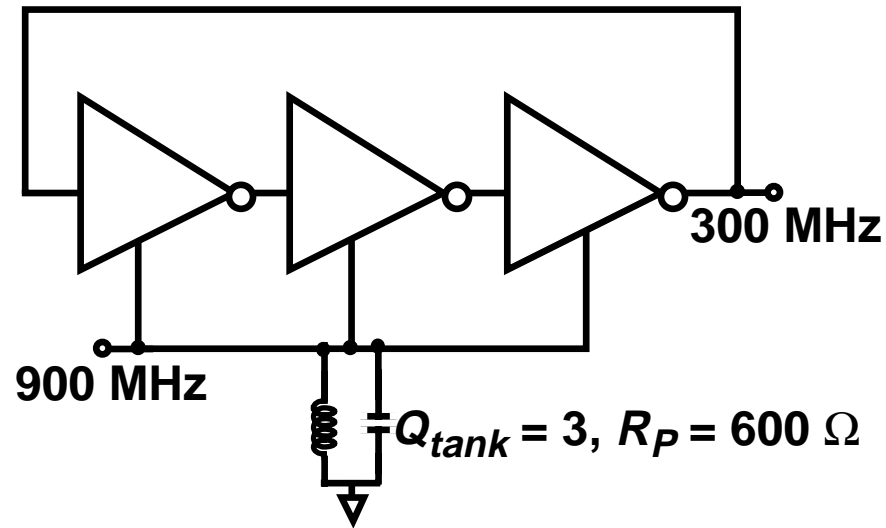


Injected Current from One Ring

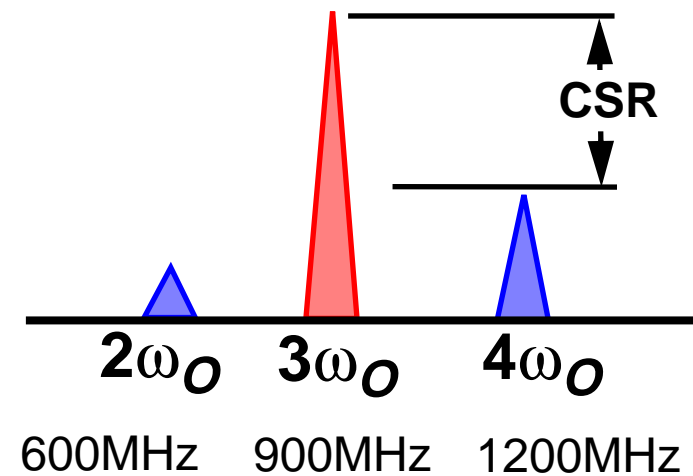
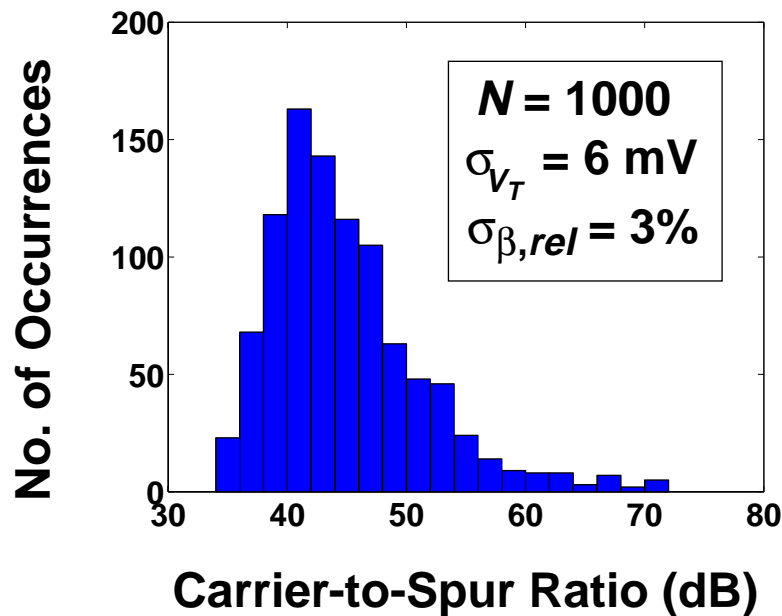


- Ideally, output spectrum contains only $3f_0$ and its harmonics.
- Due to device mismatch, spurious tones at f_0 and its harmonics appear.

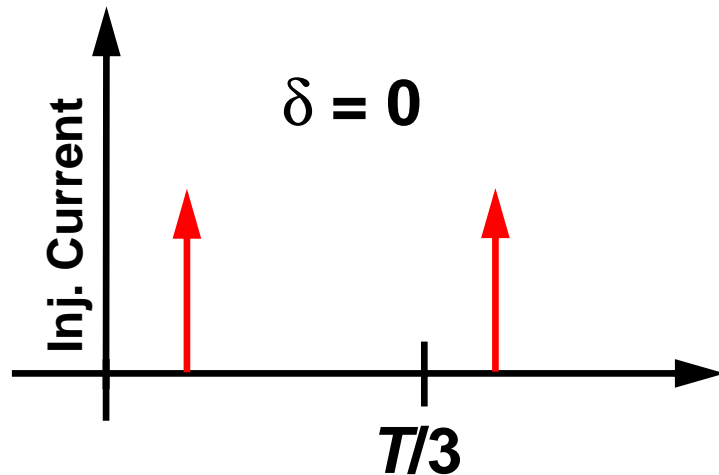
Simulated Effect of Stage Mismatch



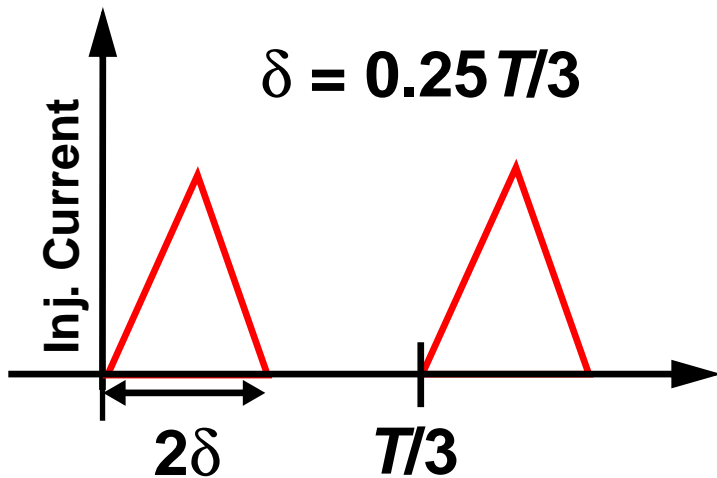
- Single-ended, three stage ring: Gaussian RV V_T and β for all NMOS devices



Output Amplitude



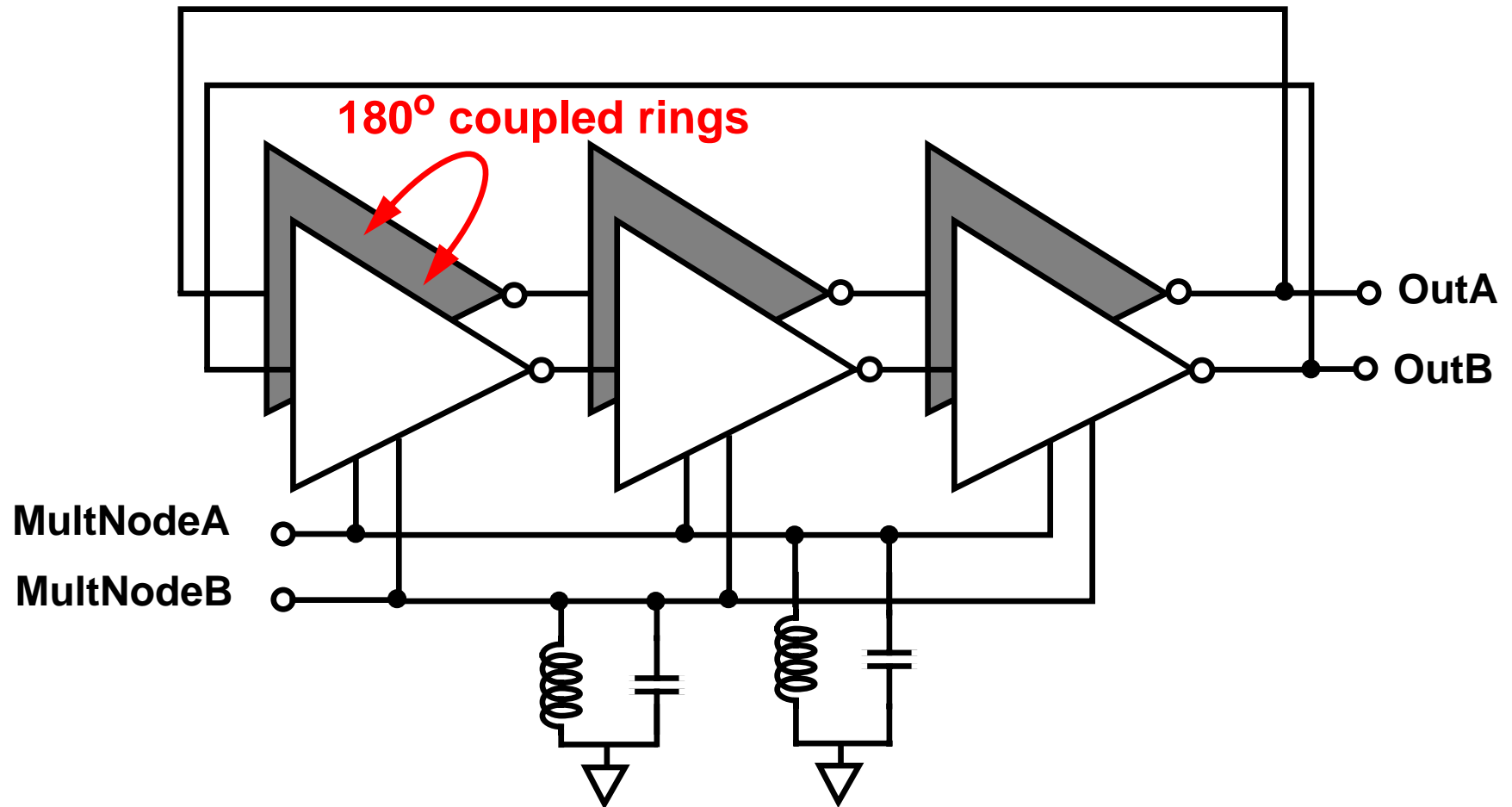
$$|V_{mult}| = 2I_{DC}R_P$$



$$|V_{mult}| = \left(\frac{4}{\pi}\right)^2 I_{DC}R_P$$

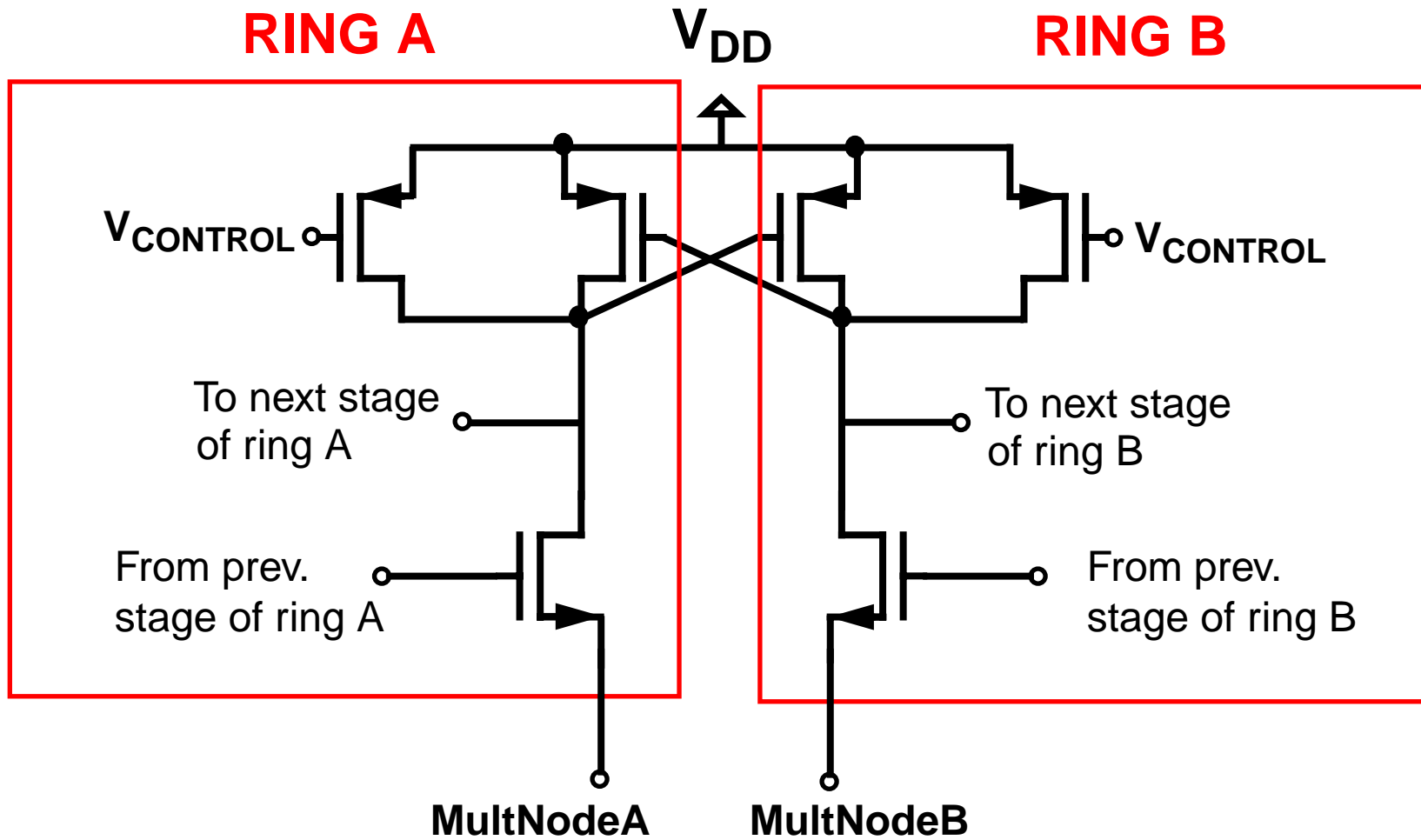
- Depends on sharpness of current injection, and DC current.

Oscillator: Differential Implementation

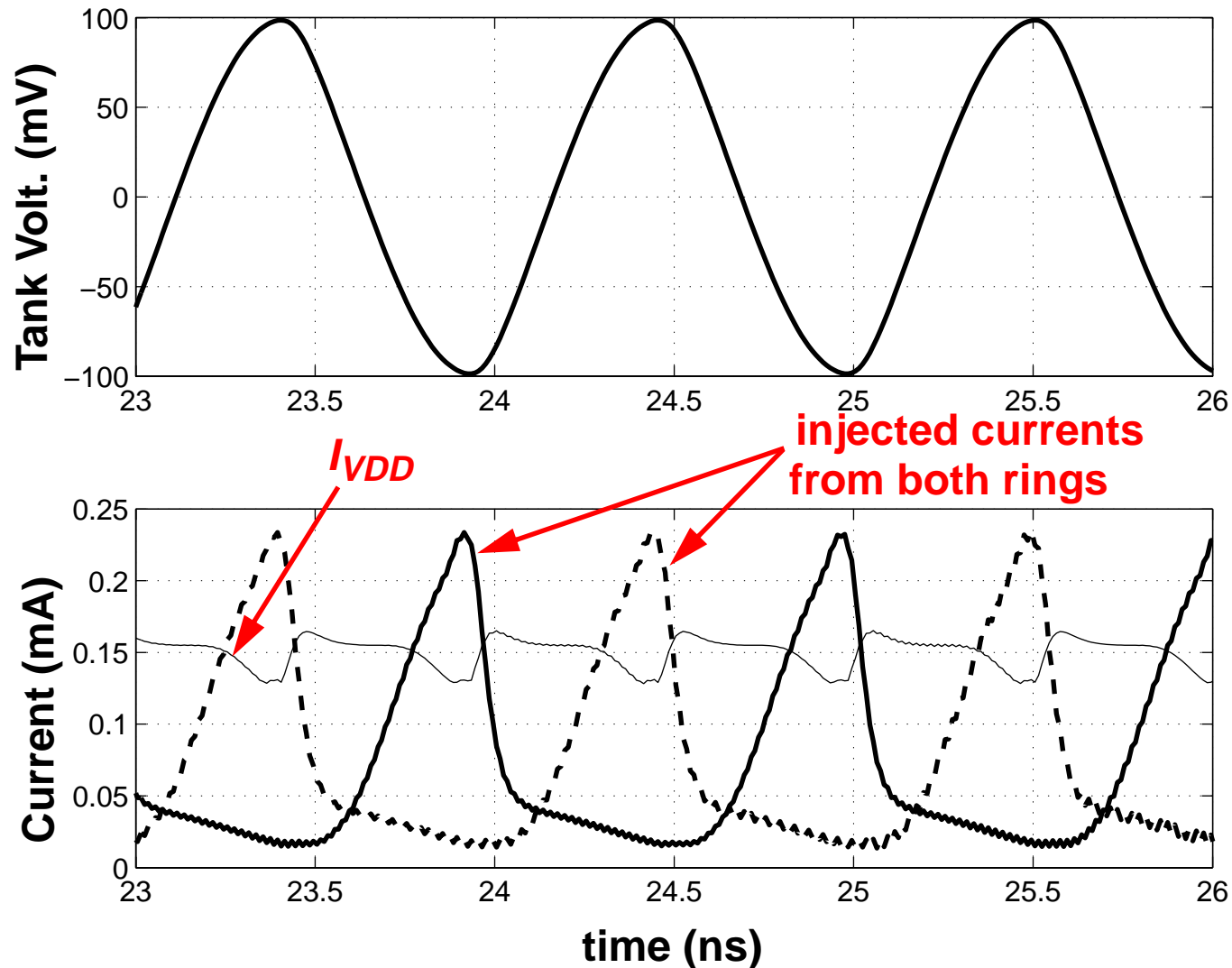


- Twice the voltage amplitude for twice the current consumption.

Interstage Coupling

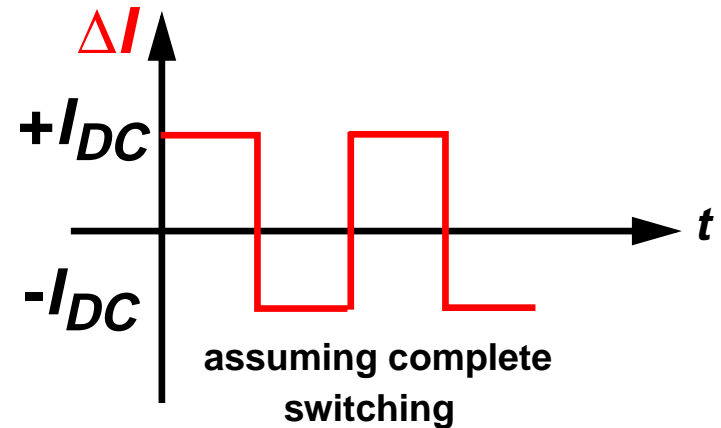
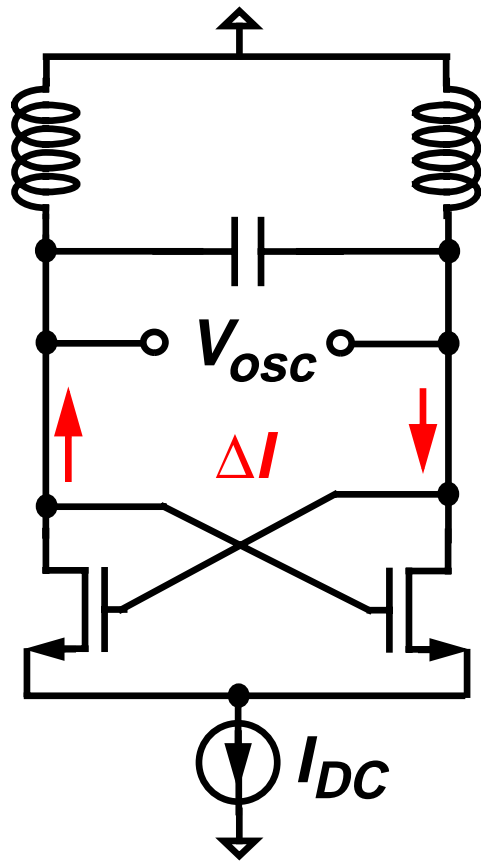


Output Amplitude: Simulation at 900 MHz



- Get 100 mV voltage swing with $I_{DC} = 150 \mu\text{A}$ and $R_P = 600 \Omega$.

Comparison: Ideal LC Oscillator

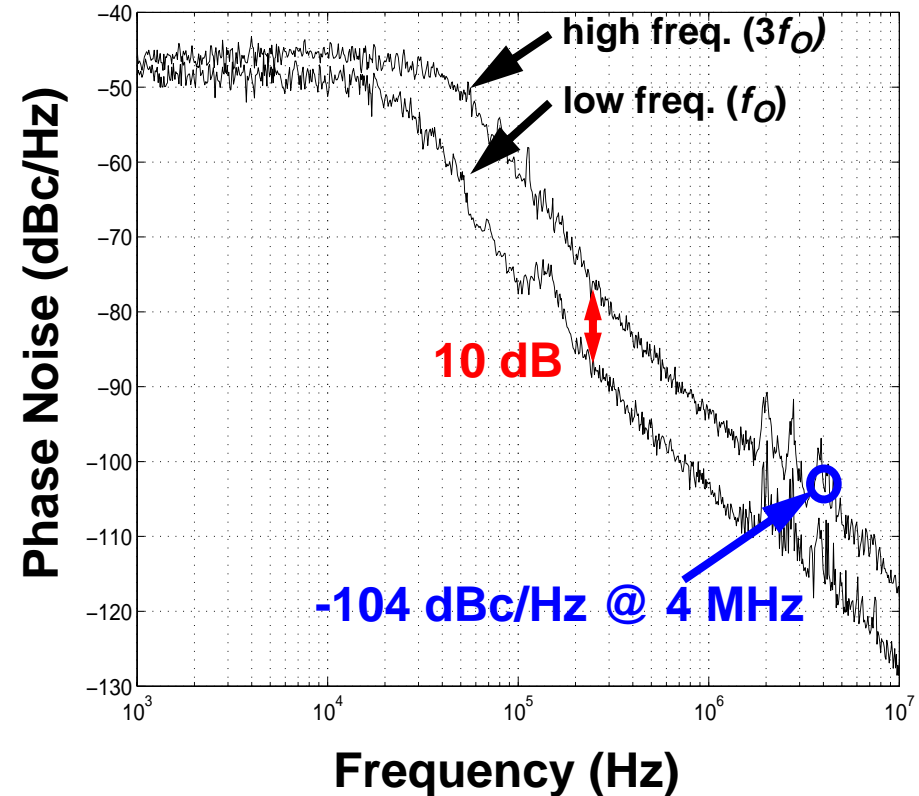
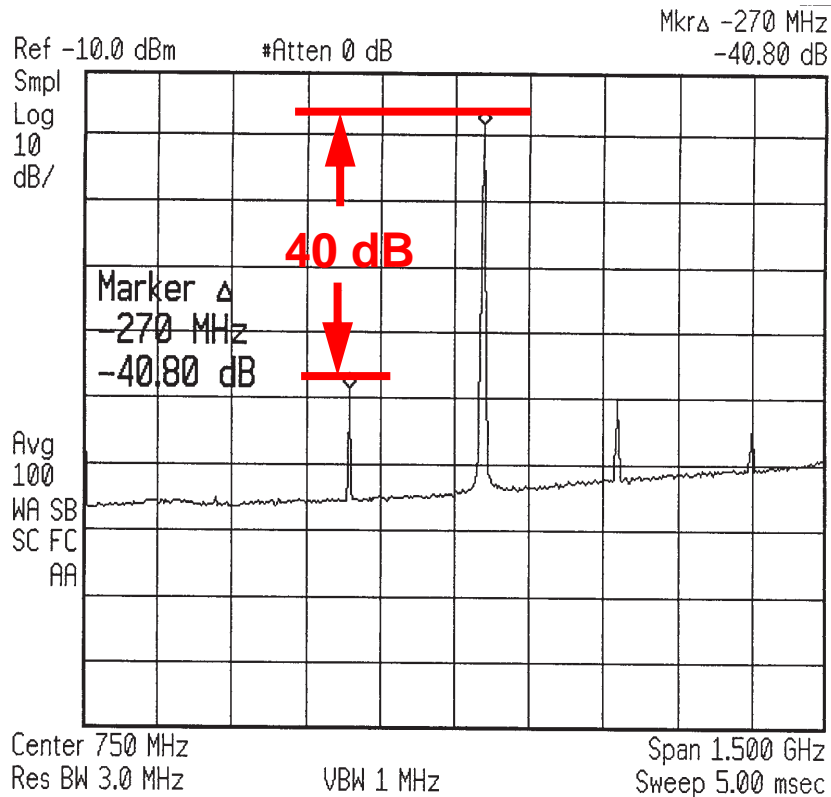


$$|V_{osc}| = \frac{4}{\pi} I_{DC} R_P$$

- LC oscillator shown would ideally provide **115 mV** voltage swing with $I_{DC} = 150 \mu\text{A}$ and $R_P = 600 \Omega$.

A Prototype VCO at 900 MHz

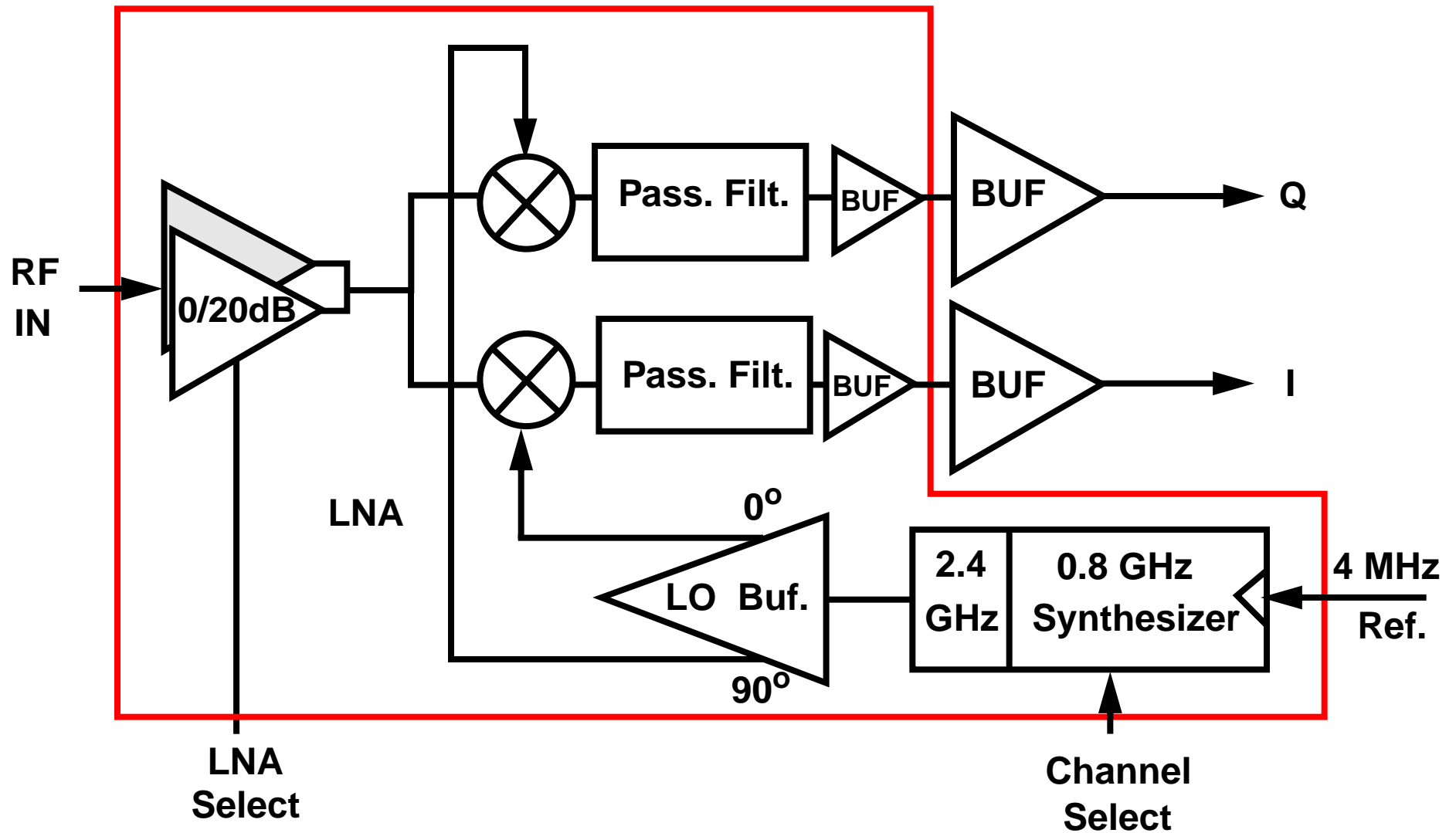
- Prototype oscillator built in 0.25 μm CMOS - providing 300 MHz and 900 MHz output frequencies.
- Operates at voltages as low as 1.3 V, while consuming 210 μA .



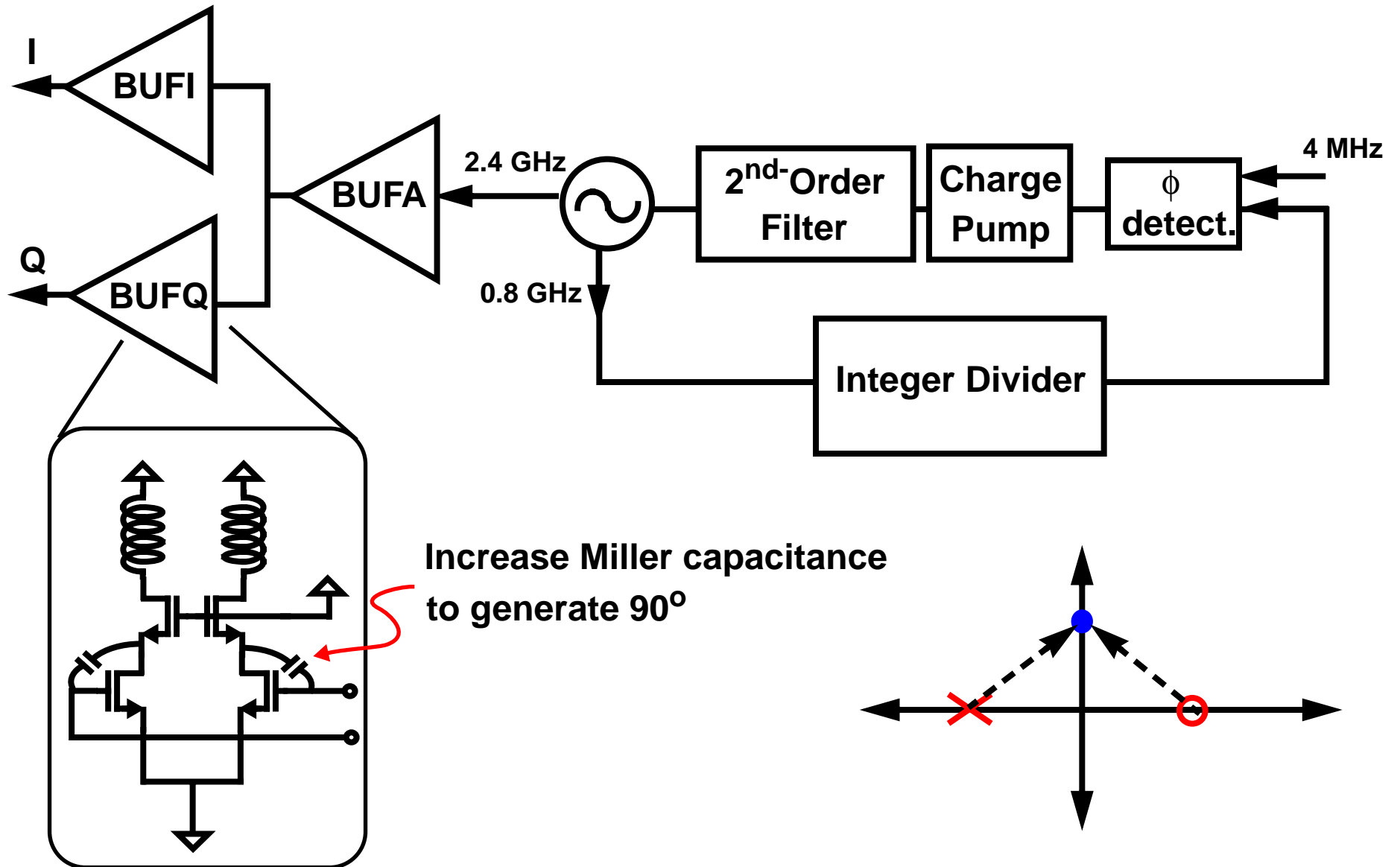
Synthesizer Design Summary

- The power consumption of the high-frequency prescaler is identified as critical.
- After studying various low-power prescaler design techniques, a new multiplier VCO is introduced.
- A prototype design has been fabricated and tested for 900 MHz operation. It trades off phase noise performance for lower power consumption.

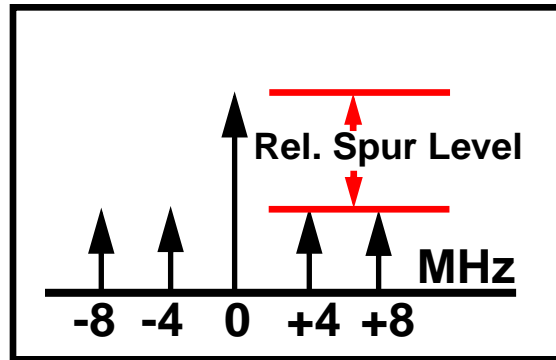
A Fully-Integrated Receiver at 2.45 GHz



LO Generation Circuits



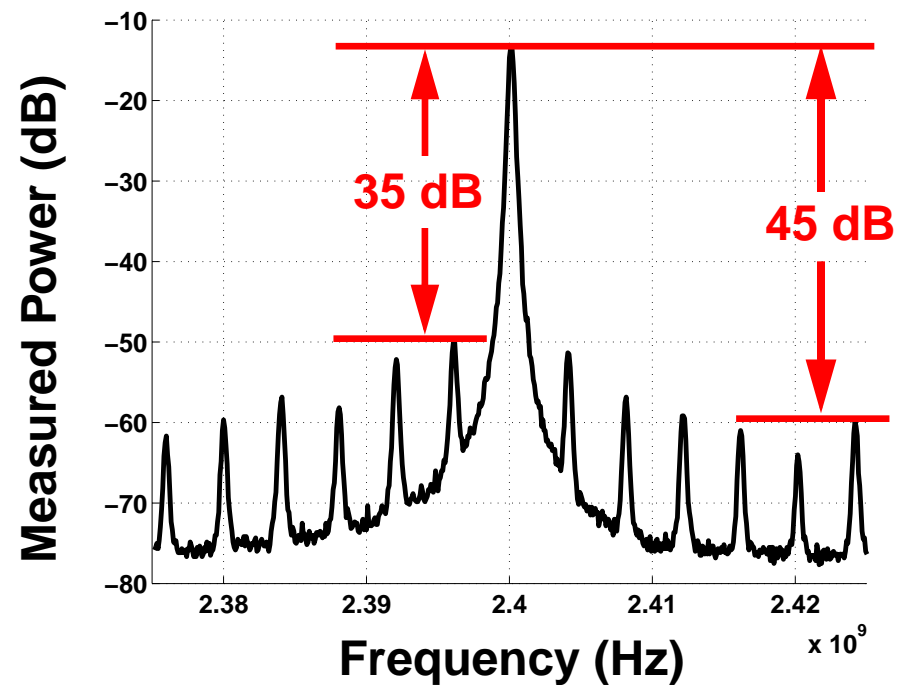
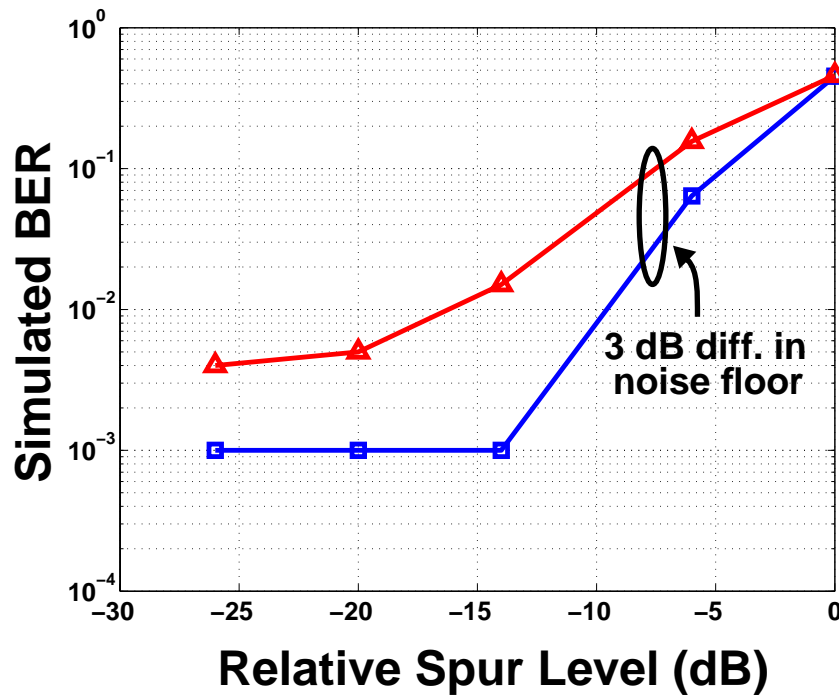
Reference Spurs: Measurements



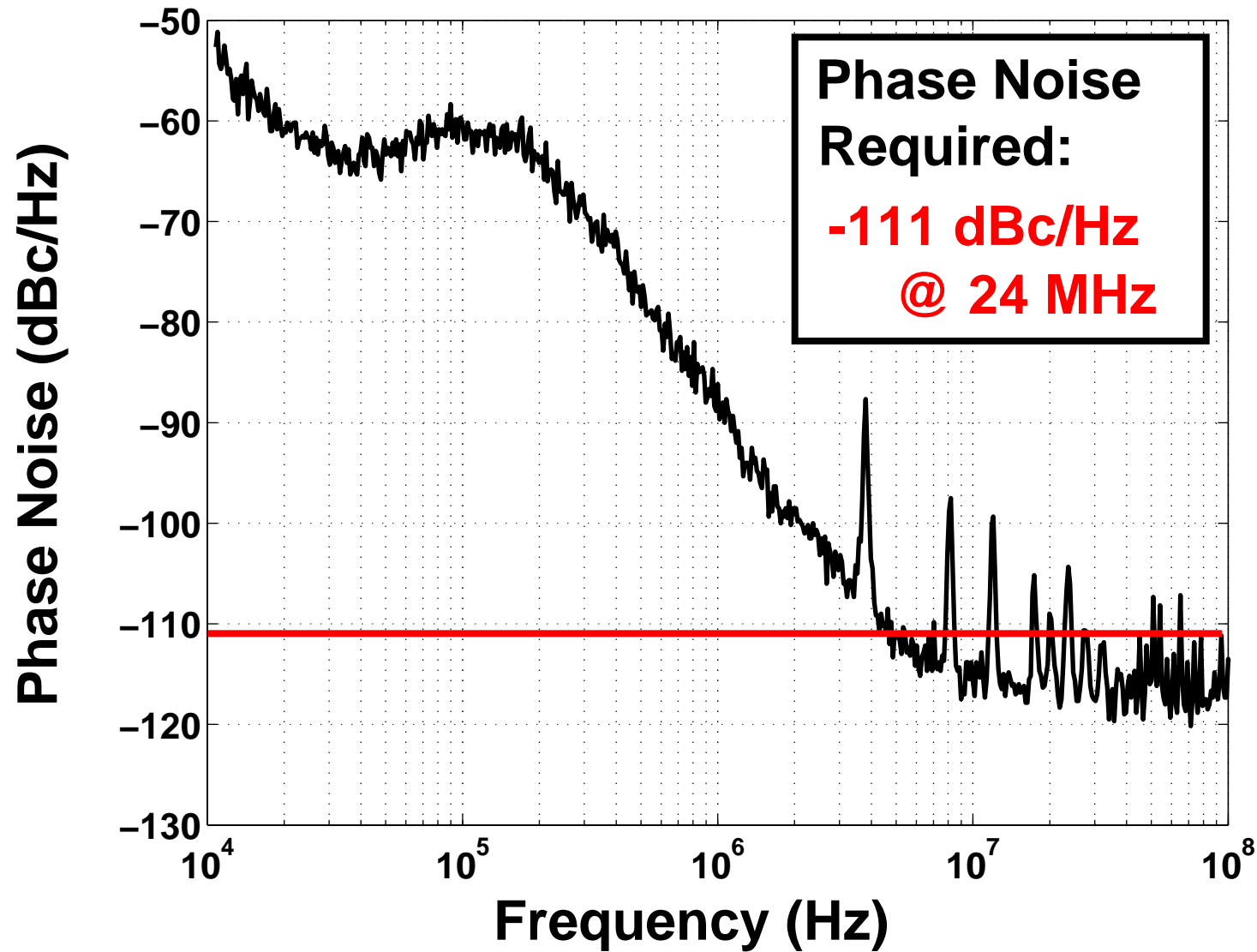
Required:

- 4 MHz, 8 MHz spurs, 20 dB below carrier.
- 24 MHz spur, 40 dB below carrier.

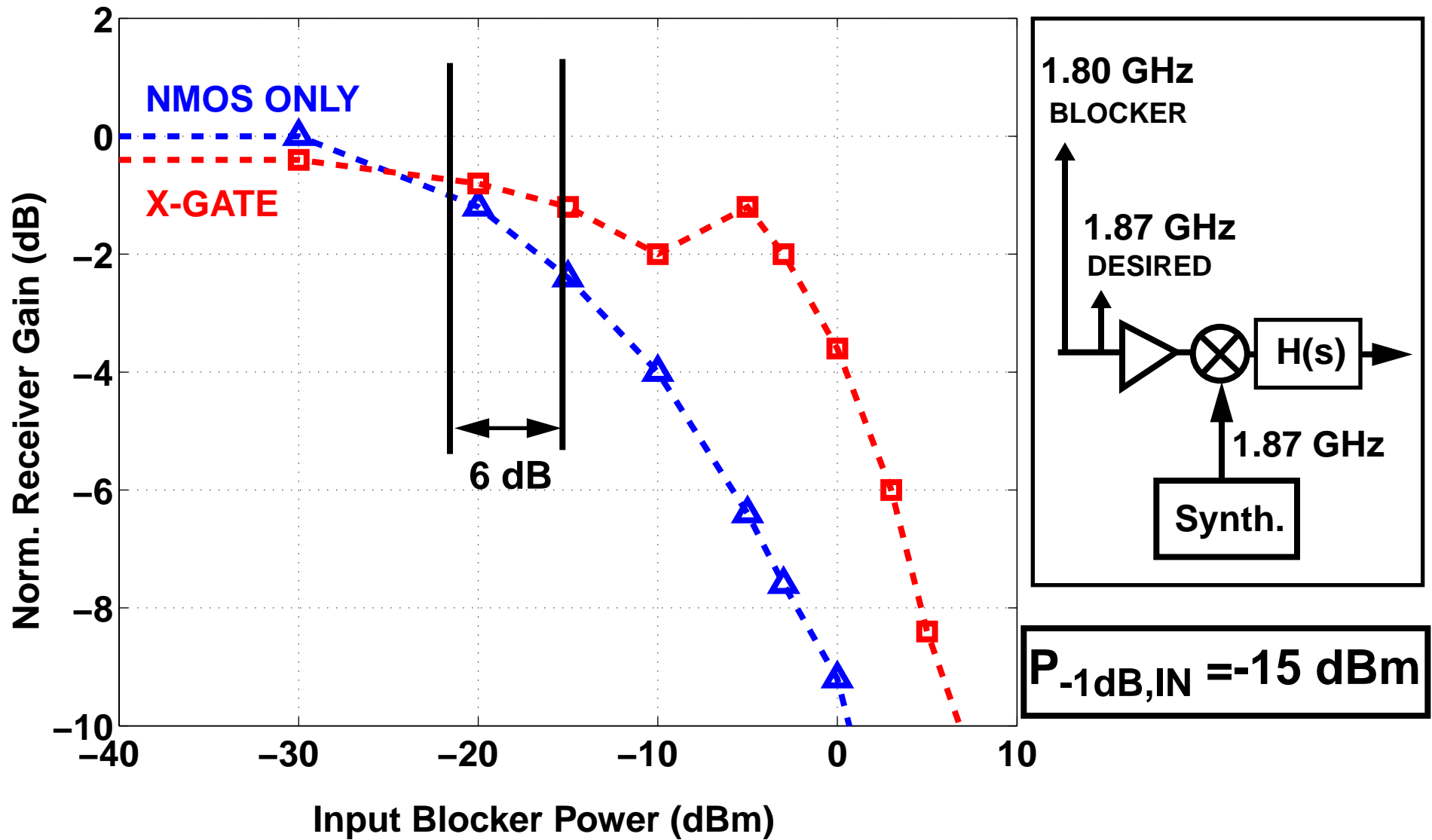
Eases charge pump design with 1.8 V supply.



Phase Noise Measurement



Blocker Sensitivity



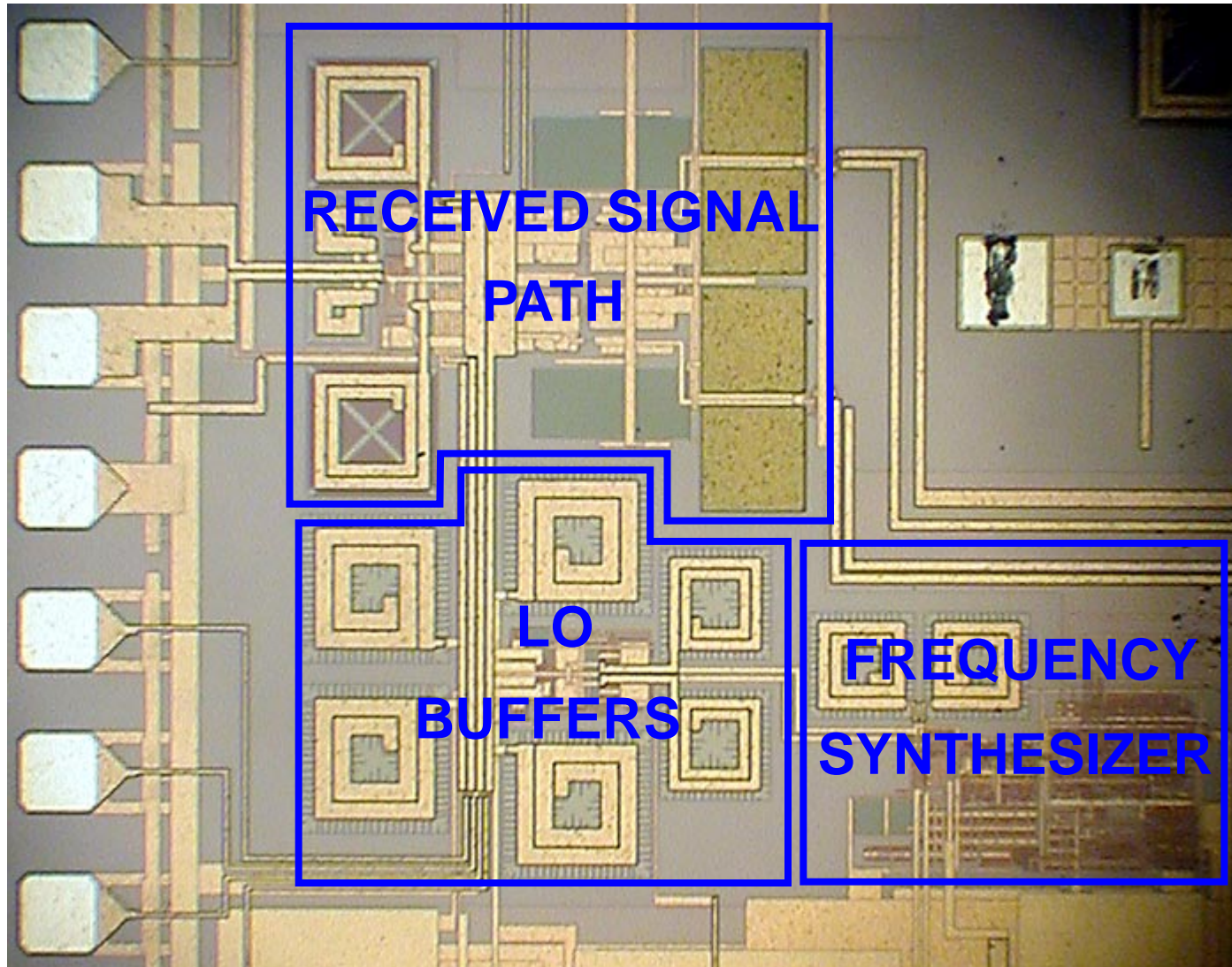
Performance Summary

Performance	Achieved	Required
Passband Noise Fig. (@1.9 GHz)	8.8 dB ^a	< 18 dB
1-dB Blocker Compress. Pt.	-15 dBm	-20 dBm ($Q_{in} = 3$)
LO Phase Noise @24 MHz	< -115 dBc/Hz	<-111 dBc/Hz
Ref. Spur @24 MHz	-45 dBc	< -40 dBc
Signal Path Current	3 mA	
Synth. Current @2.45 GHz	2.5 mA	
LO Buffer Current	4 mA	
Total Current	9.5 mA	
Supply Voltage	1.8 V	
Active Chip Area	0.66 mm ²	
Off-chip Components	Inductor (ant.), crystal	
Technology	0.25 μ m CMOS	

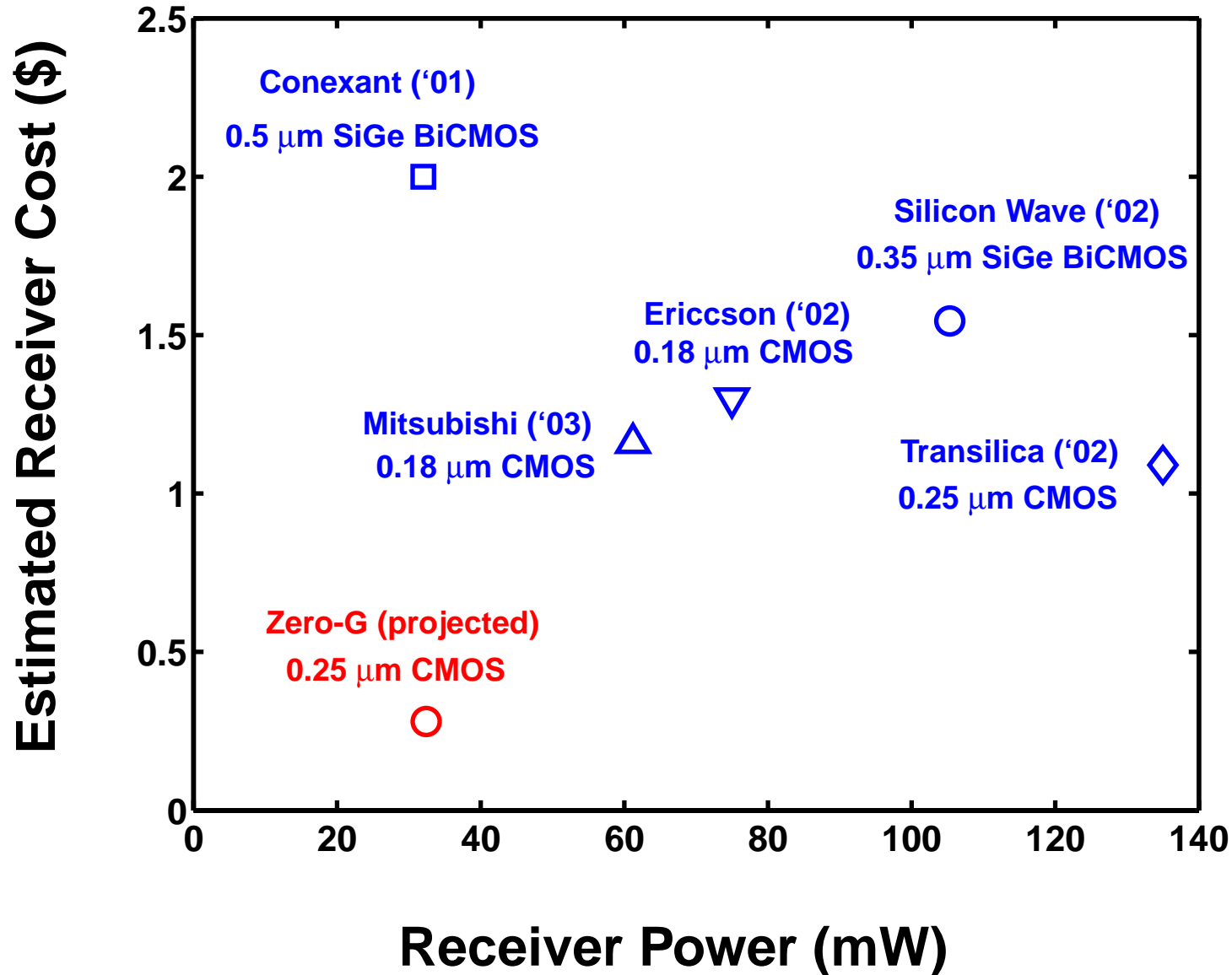
a. VGA needed after passive chain - not included in design.

Receiver Die Photo

- Implemented in 0.25 μm CMOS.



Receiver Cost-Power Comparison



Contributions

- Contributed to the concurrent design of the system specifications and circuits for the Zero-G system.
- Implemented a highly-integrated, low-power, low-cost receiver frontend which:
 - eliminates the band-select filter.
 - linearly downconverts and filters strong blockers.
 - implements a low-power synthesizer with a multiply-by-3 oscillator.
- Created and experimentally verified a unified model for injection-locked frequency dividers.

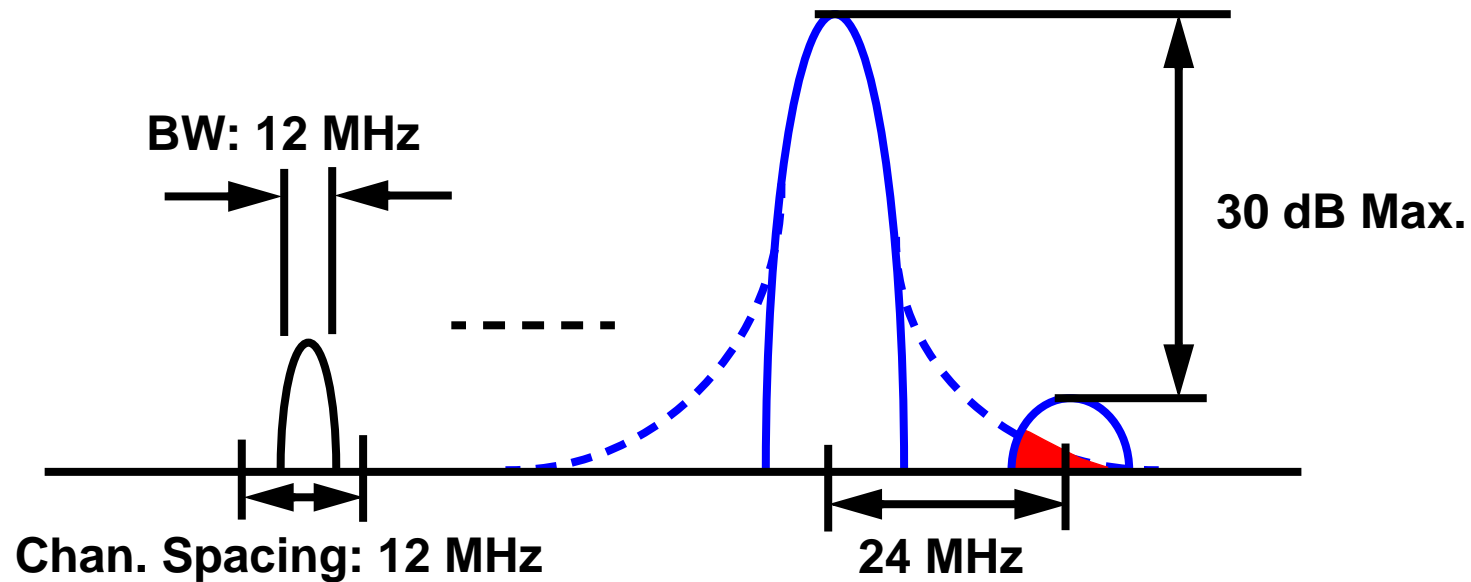
Publications

- R. J. Betancourt-Zamora, S. Verma, T. H. Lee, "**1-GHz and 2.8-GHz CMOS Injection-Locked Ring Oscillator Prescalers**," *Symposium on VLSI Circuits*, June 14-16, 2001.
- S. Verma, H. Rategh, and T. H. Lee, "**A Unified Model for Injection-Locked Frequency Dividers**," *IEEE Journal of Solid-State Circuits*, Volume 38, Issue 6, June 2003, pp 1015-1027.
- S. Verma, J. Xu, T.H. Lee, "**A Multiply-by-3 Coupled-Ring Oscillator for Low-power Frequency Synthesis**," *Symposium on VLSI Circuits*, June 12-14, 2003, pp 189-192.
- M. Hamada, S. Verma, J. Xu, T.H. Lee, "**Completely DC-free Direct Sequence Spectrum Spreading Scheme for Low Power, Low Cost, Direct Conversion Transceiver**," *WNCG Wireless Networking Symposium*, October 2003.
- S. Verma, J. Xu, T.H. Lee, "**A Multiply-by-3 Coupled-Ring Oscillator for Low-power Frequency Synthesis**," *IEEE Journal of Solid-State Circuits*, Volume 39, Issue 4, April 2004, pp 709-713
- S. Verma, J. Xu, M. Hamada, T.H. Lee, "**A Low-Cost, Low-Power Wireless Receiver**," *IEEE Journal of Solid-State Circuits*, under preparation.

Acknowledgments

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- Ann Guerra
- SMIrC group, Prof. Wooley's group, Prof. Wong's group
- Mototsugu Hamada and Junfeng Xu
- National Semiconductor, Stanford Graduate Fellowships
- Friends!
- Family

Phase Noise Requirement



- Required SNR = $\underbrace{-30}_{\text{Signal}} \underbrace{-[10\log(12\text{MHz}) + L(24\text{MHz})]}_{\text{Phase Noise from Interferer}}$

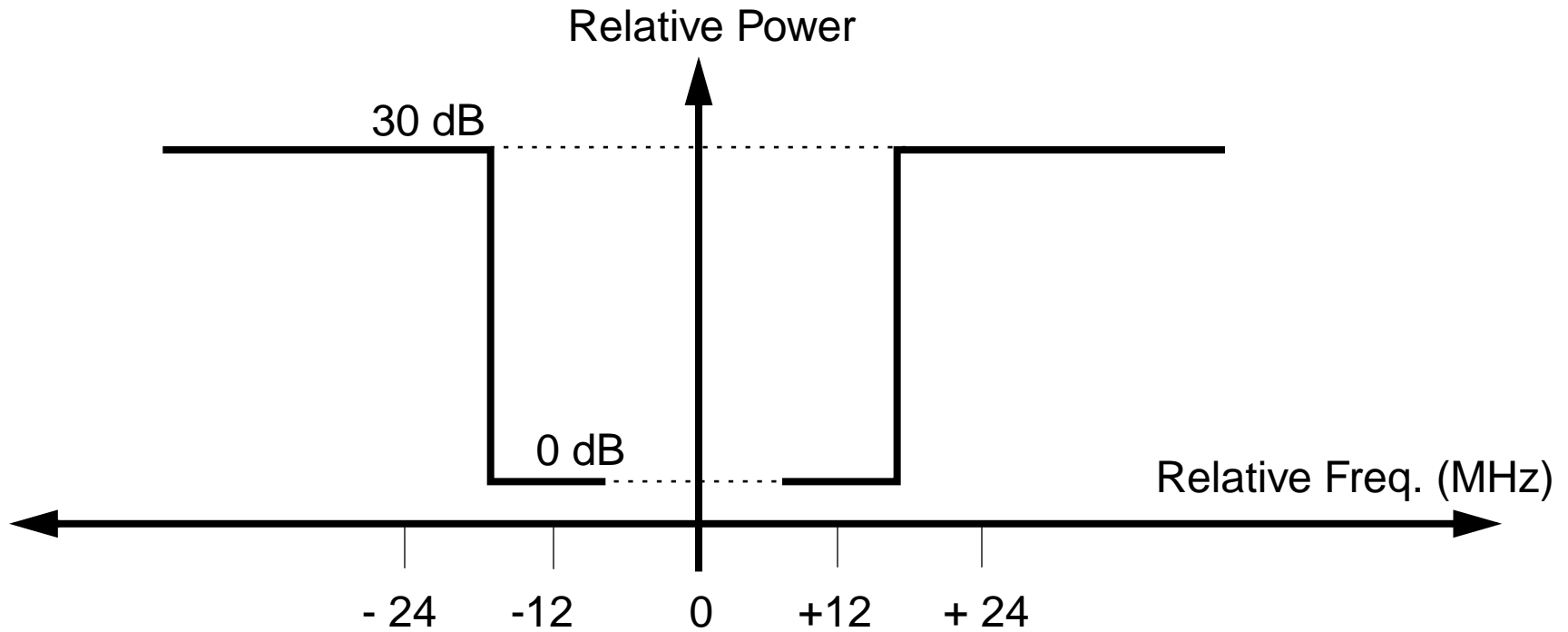
> 10 dB

- $L(24 \text{ MHz}) < -110.8 \text{ dBc/Hz}$

I-Q Mismatch

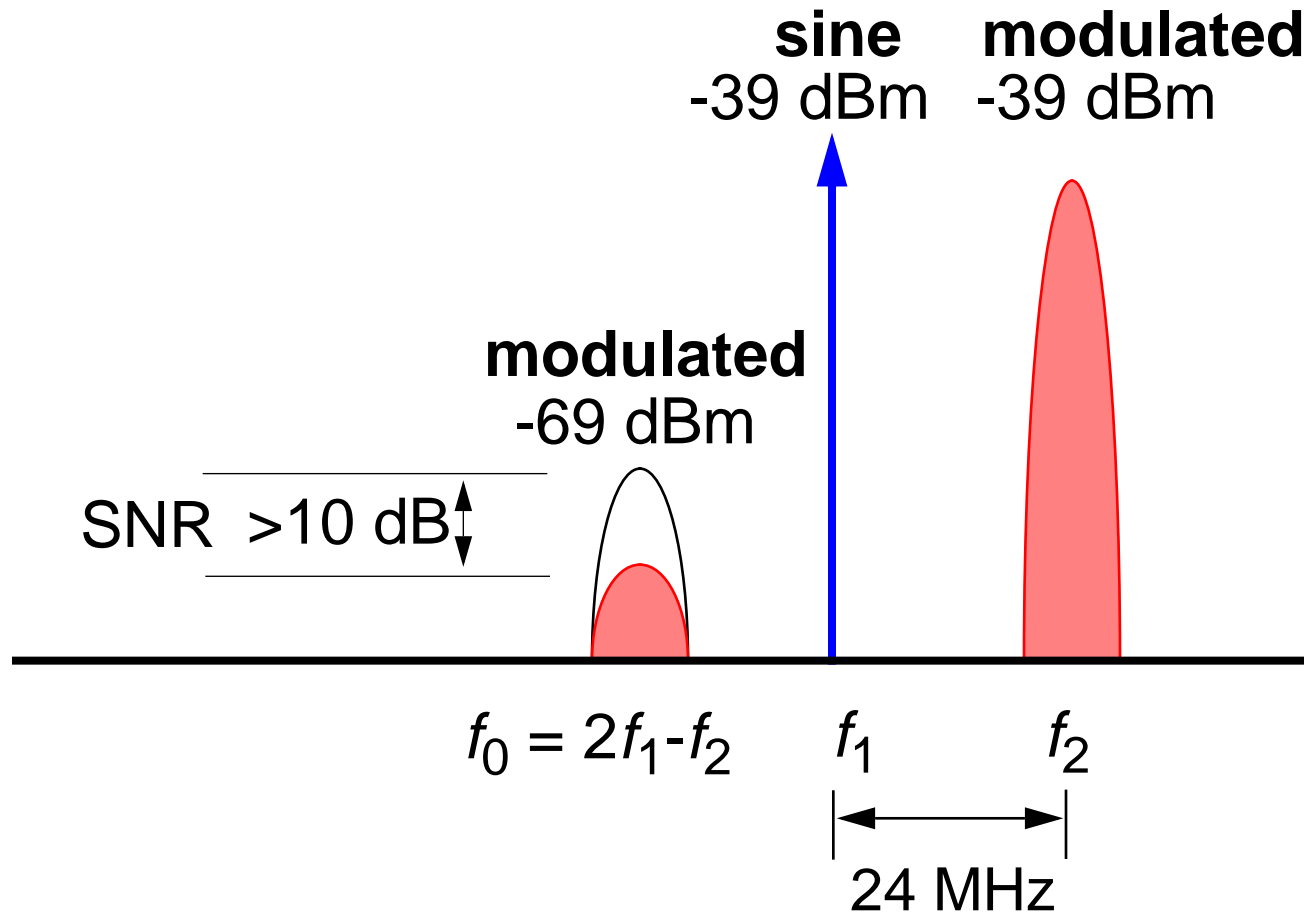
- **Gain mismatch:** for a gain mismatch of α , SNR degrades by α^2 .
 - 10% mismatch brings 0.9 dB of SNR degradation.
- **Phase mismatch:** for a phase mismatch of ϕ , signal power reduced to $1/(1+\phi)$ in the worst case.
 - 10° mismatch brings 0.7 dB SNR degradation.

Receiver In-band Blocking



- Relaxed adjacent and alternate channel requirement.
- Eases phase noise and IIP3 required from the receiver.

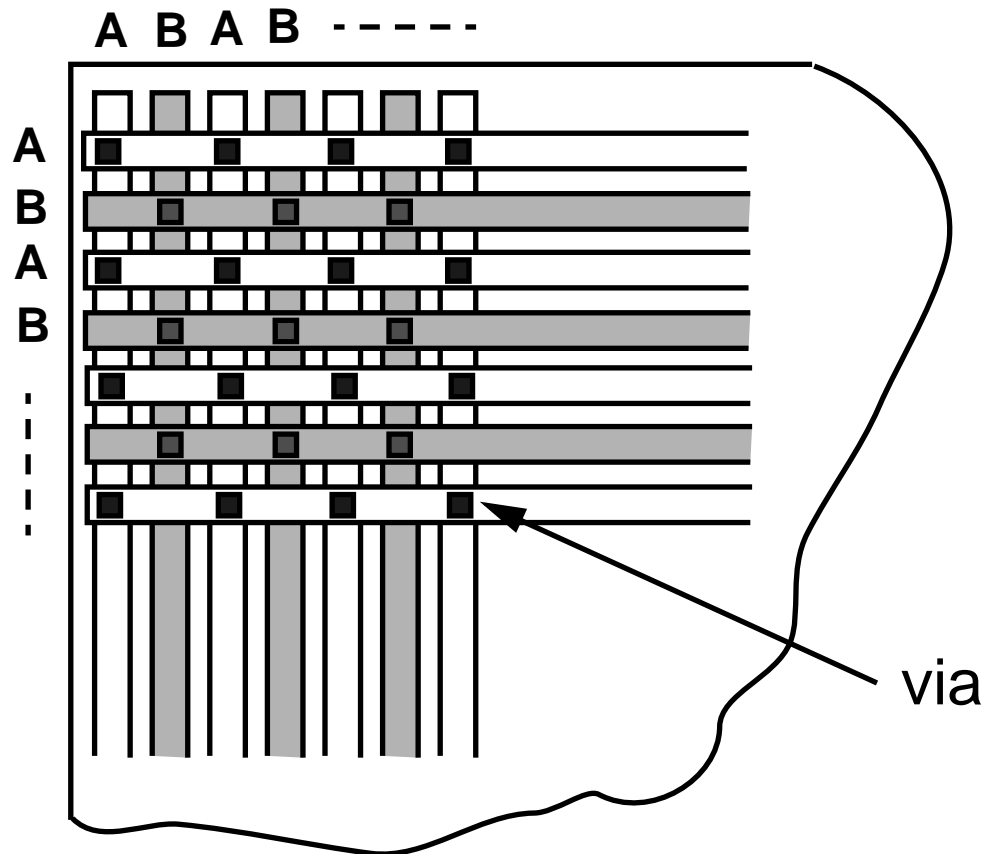
Second/Third-Order Intercept



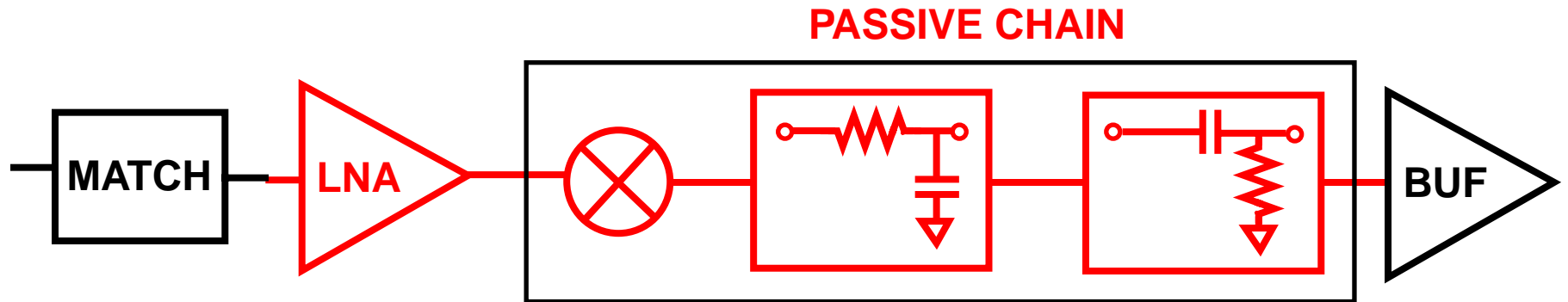
- IIP3 required is -19 dBm, limited by end buffers.
- IIP2 required is +1 dBm, limited by input symmetry.

High-Density Capacitors

- Woven structure of M1-M2-M3-M4-M5 lines on top of poly-poly capacitors.



Receive Path Gain/Power Distribution

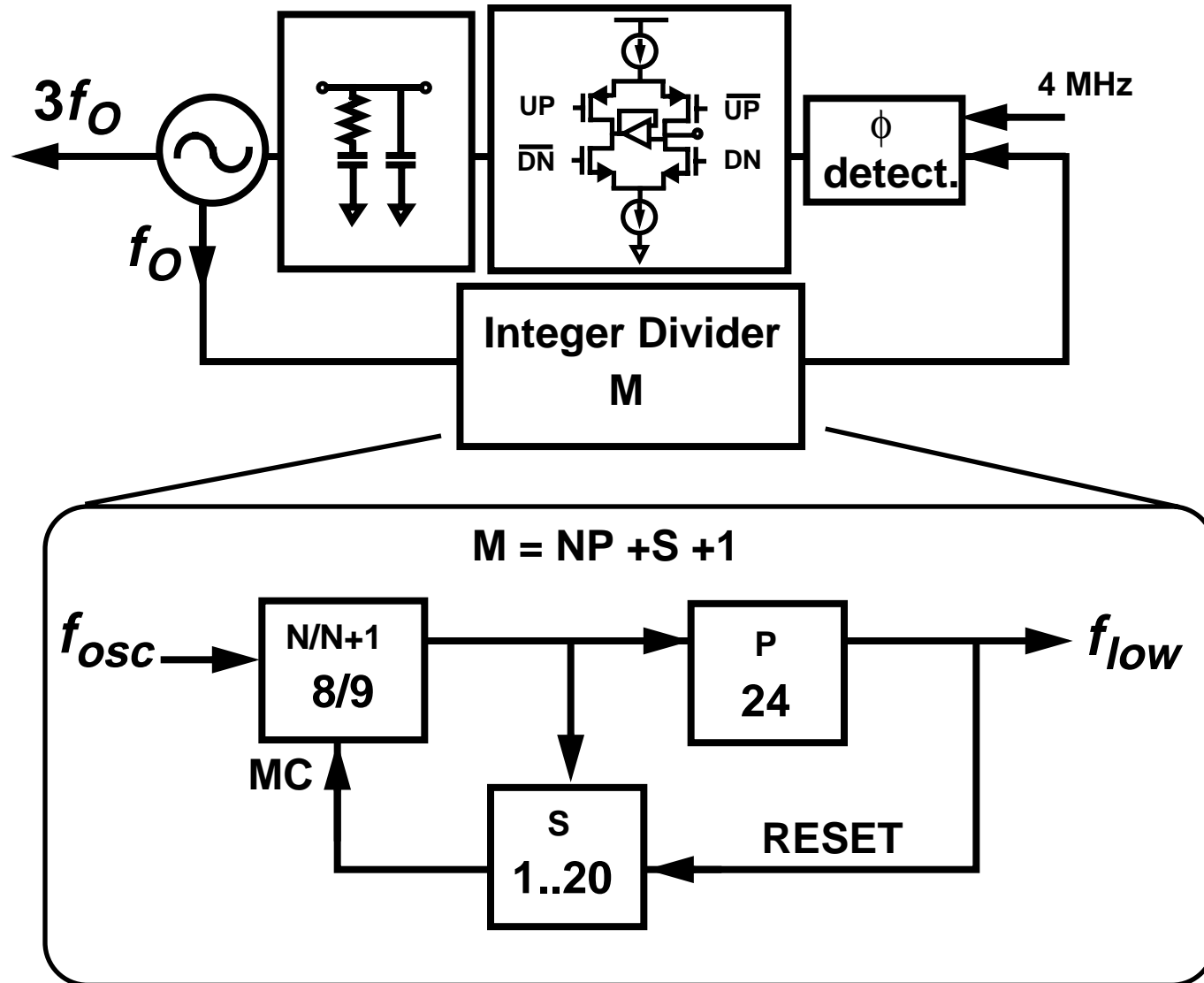


NF	2.1 dB	4 dB	16 dB	1.5 dB
G_{AV}	-2.1 dB	9 dB	-16 dB	

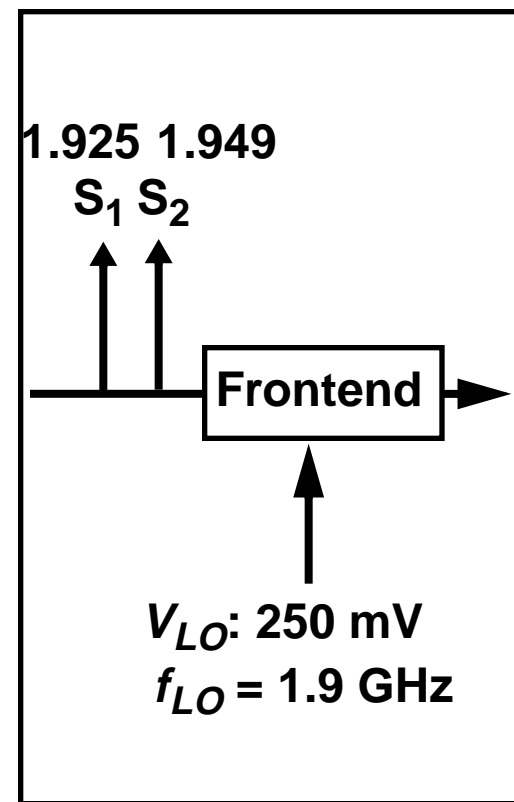
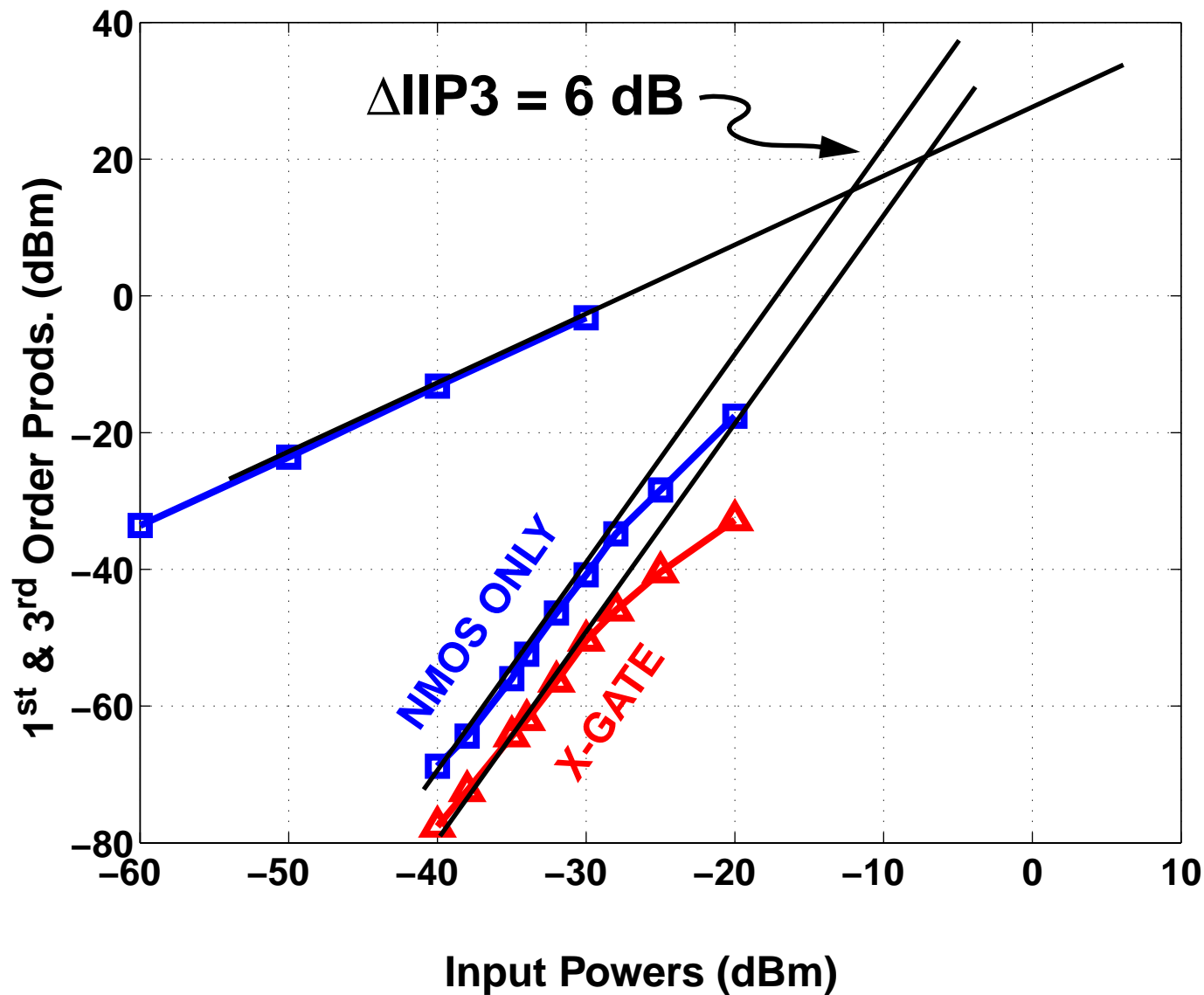
Cumulative NF = 13.9 dB

System NF = 8.8 dB

PLL Implementation

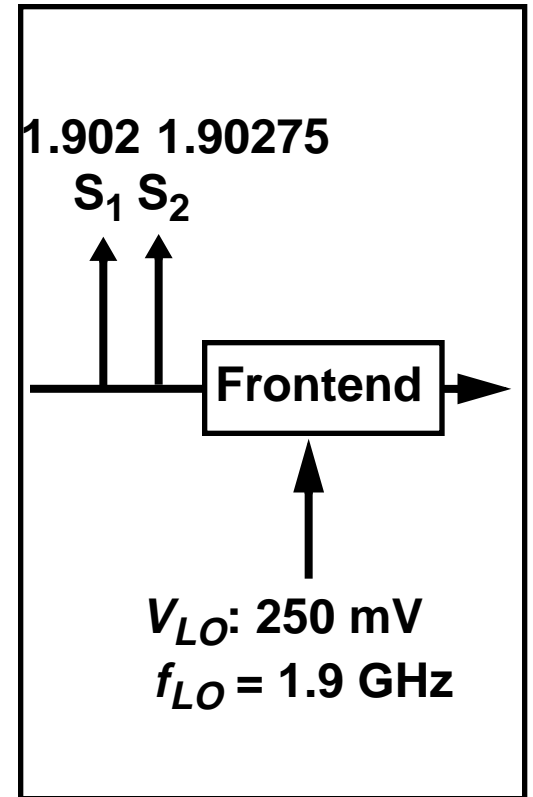
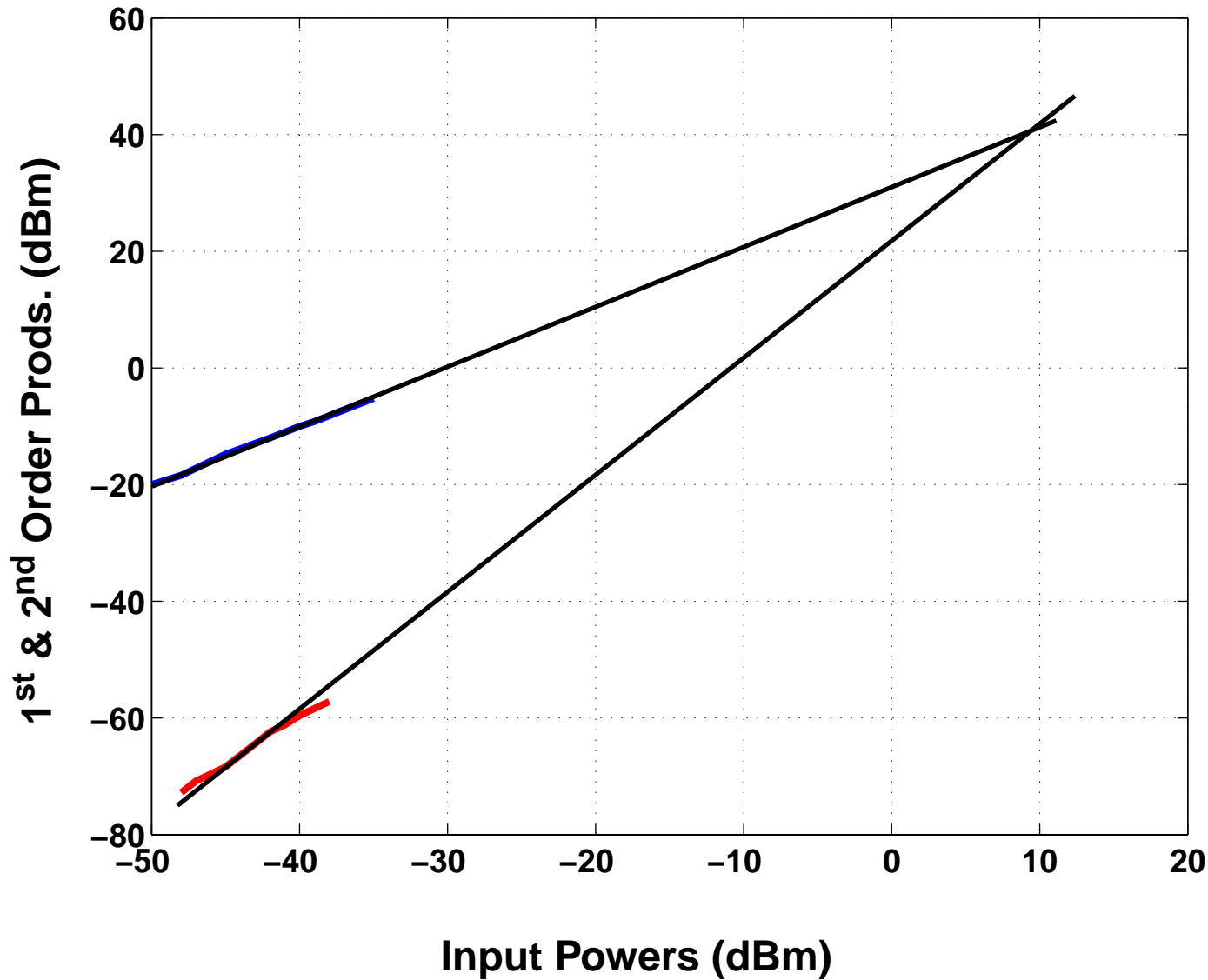


Alternate Channel IIP3 (External LO)



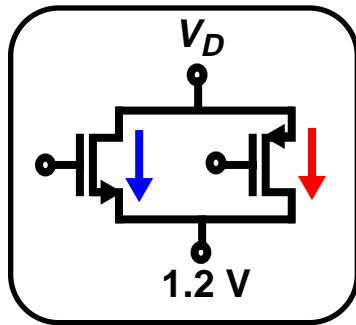
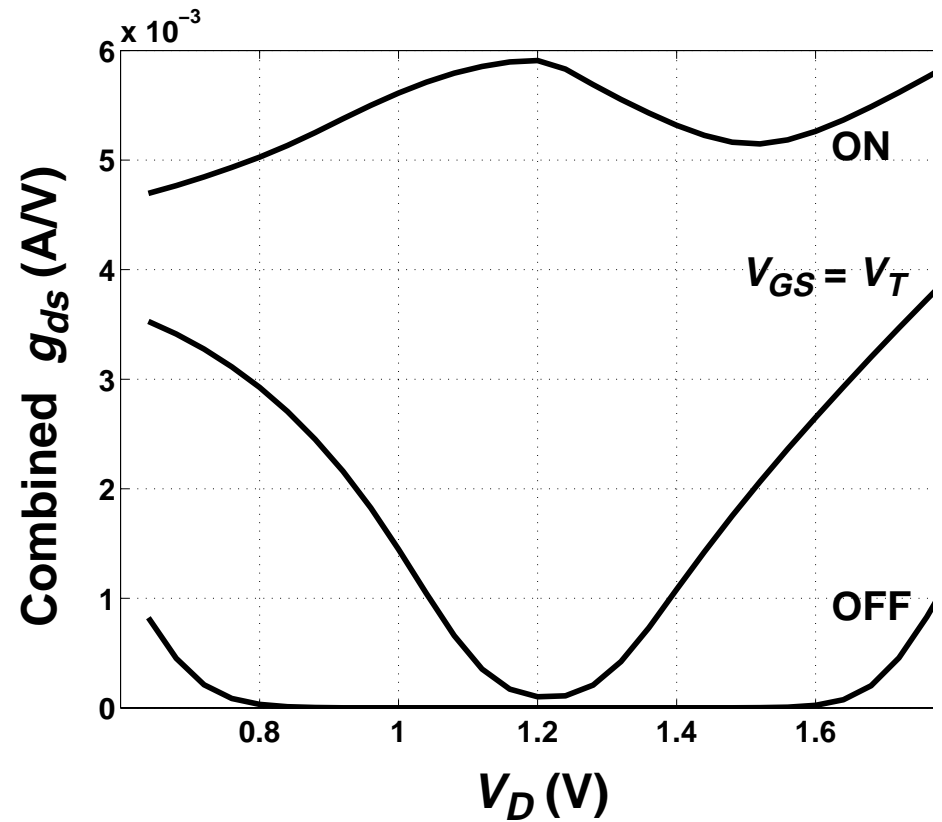
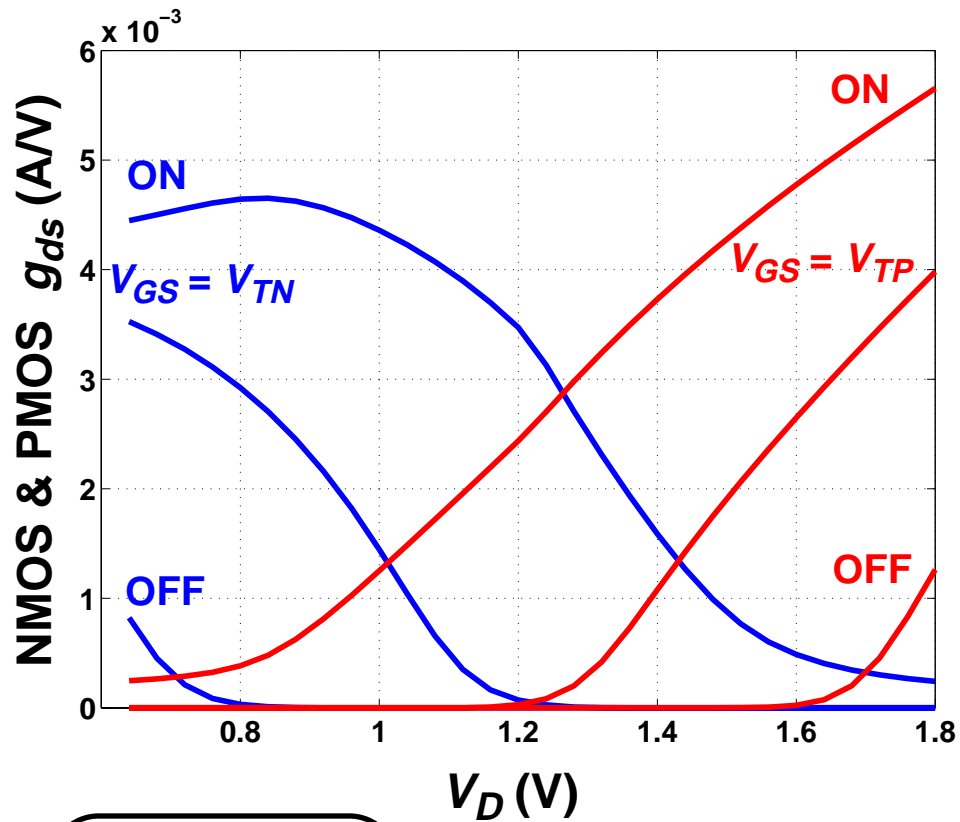
IIP3 = -7 dBm

IIP2 (External LO)



IIP2 = 10 dBm

X-Gate Mixer (III): DC Simulations



Cost/Power Estimation Assumptions

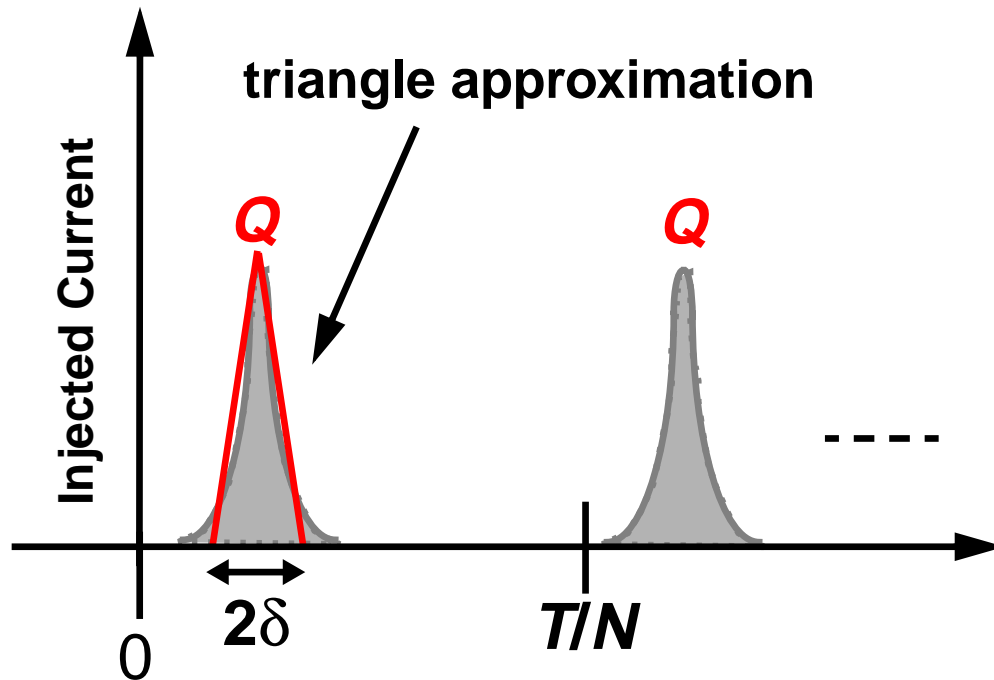
- SAW filter after antenna = **\$0.30**
- Crystal: +/- 10 ppm = **\$0.25**; +/- 100 ppm = **\$0.15**
- T/X Switch = **\$0.50**
- RF Balun = **\$0.05**
- Passives = **\$0.01** each (ignored)
- Cost of CMOS = **\$0.10/mm²**, SiGe BiCMOS = **0.15/mm²**
- Our work :

projected receiver power = $2 \times (9.5 \text{ mA} \times 1.8) = \mathbf{34.2 \text{ mW}}$

projected Si area = $2 \times (0.66 \text{ mm}^2) = \mathbf{1.3 \text{ mm}^2}$

No T/X switch, No SAW filter, +/- 100 ppm crystal.

Output Amplitude: Calculation



Fourier coefficient at $2N\pi/T$:

$$|c_1| = \frac{NQ}{T} \cdot 2 \left[\frac{\sin(N\pi\delta/T)}{(N\pi\delta/T)} \right]^2$$

Using $I_{DC} = NQ/T$ and $Z_{tank} = R_P$,

$$|V_{mult}| = 2 \left[\frac{\sin(N\pi\delta/T)}{(N\pi\delta/T)} \right]^2 I_{DC} R_P$$